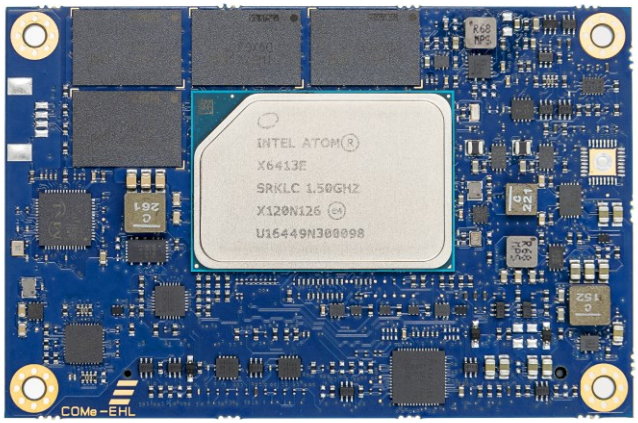
COME TYPE10 EHL HW MANUAL



COMe Type 10 Compliant

Revision history

DATE	REVISION	CHANGE DESCRIPTION
16/02/2023	1.0.0	Release
21/02/2023	1.0.1	Corrected refuse on Power Sequence. Added Boot Mode Chapter

TABLE OF CONTENTS

CHAPTER 1

1. INTRODUCTION

This Chapter gives background information on this document.
Section includes :

- Acronyms and Abbreviations Used
- Signal Table Terminology
- Document and Standard References

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

Cells with grey text contain information that is not supported on this board.

This document also contains samples reference schematics for different interfaces.

COMe EHL module may not feature the full set of all interfaces that defined in COMe specification.

An evaluation carrier is available for COMe EHL computer on module.

All examples of this document are based on COMe EHL carrier board that is available from ENGICAM. This document also provides a collection of useful documentation, application reports, and design recommendations.

The last part of the document reports the main features of the BIOS setup.

1.1 ACRONYMS AND ABBREVIATIONS USED

The table below shows the acronyms and abbreviations used in the manual.

ABBREVIATION	EXPLANATION
ADC	Analogue to Digital Converter
Auto-MDIX	Automatically Medium Dependent Interface Crossing, a PHY with Auto-MDIX f is able to detect whether RX and TX need to be crossed (MDI or MDIX)
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CPU	Central Processor Unit
DAC	Digital to Analogue Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor
DSI	Display Serial Interface
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
HDA	High Definition Audio (HD Audio), digital audio interface between CPU and audio codec
HDMI	High-Definition Multimedia Interface, combines audio and video signal
I2C	Inter-Integrated Circuit, two wire interfaces for connecting low speed peripherals
I2S	Integrated Interchain Sound, serial bus for connecting PCM audio data between two devices
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signalling, electrical interface standard that can transport very high speed signals over twisted-pair cables.
MSB	Most Significant Bit
NA	Not Available
NC	Not Connected
OD	Open Drain
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation

ABBREVIATION	EXPLANATION
RGB	Red Green Blue, colour channels in common display interfaces
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SOC	System on a Chip, IC which integrates the main component of a computer on a single chip
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
USB	Universal Serial Bus, serial interface for internal and external peripherals

1.2 SIGNAL TABLE TERMINOLOGY

The Table below describes the terminology used in this section for the Signal Description tables.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

DIRECTION	TYPE	NOTE
Input		Input to the Module
Output		Output from the Module
Output OD		Open drain output from the Module
Bi-Dir		Bi-directional signal (can be input or output)
Bi-Dir OD		Bi-directional signal; output from the Module is open drain
Diff100		Differential 100 Ohm
Diff90		Differential 90 Ohm
	VDD_IN	Module input voltage
	CMOS 1.8V	CMOS logic input and / or output, 1.8V I/O supply level or tolerance
	CMOS 3.3V	CMOS logic input and / or output, 3.3V I/O supply level or tolerance
	CMOS VDD_IO	CMOS logic I/O level – set to 1.8V for COMe EHL
	CMOS VDD_JTAG_IO	VDD_JTAG_IO is 1.8V in COMe EHL. The JTAG emulator adjusts to the VDD_JTAG_IO level provided by the Module, on the JTAG connector
	GBE MDI	Differential analog signalling for Gigabit Media Dependent Interface
	GPIO PU	All GPIOs have programmable internal pull-up (20kOhm nominal) and pull-down (20kOhm nominal) resistor which are off by default.

1.3 DOCUMENT AND STANDARD REFERENCES

1.3.1 EXTERNAL INDUSTRY STANDARD DOCUMENTS

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now INTEL) (www.INTEL.com).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now INTEL) (www.INTEL.com).
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org).
- PICMG® EEEP Embedded EEPROM Specification, Rev. 1.0, August 2010 (www.picmg.org).
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org).
- SPI Bus – "Serial Peripheral Interface" - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).
- USB Specifications (www.usb.org).

1.3.2 PICMG® COM.0 DOCUMENTS

COM Express® Module Base Specification Rev 3.0

1.4 NON-INTENDED USE

WARNING

Use the COMe module in the specified temperature ranges only!
Use the COMe module in the specified humidity ranges only!

1.5 ELECTROSTATIC SENSITIVE DEVICE

The ENGICAM COMe module is an electrostatic sensitive device and it is packed accordingly.

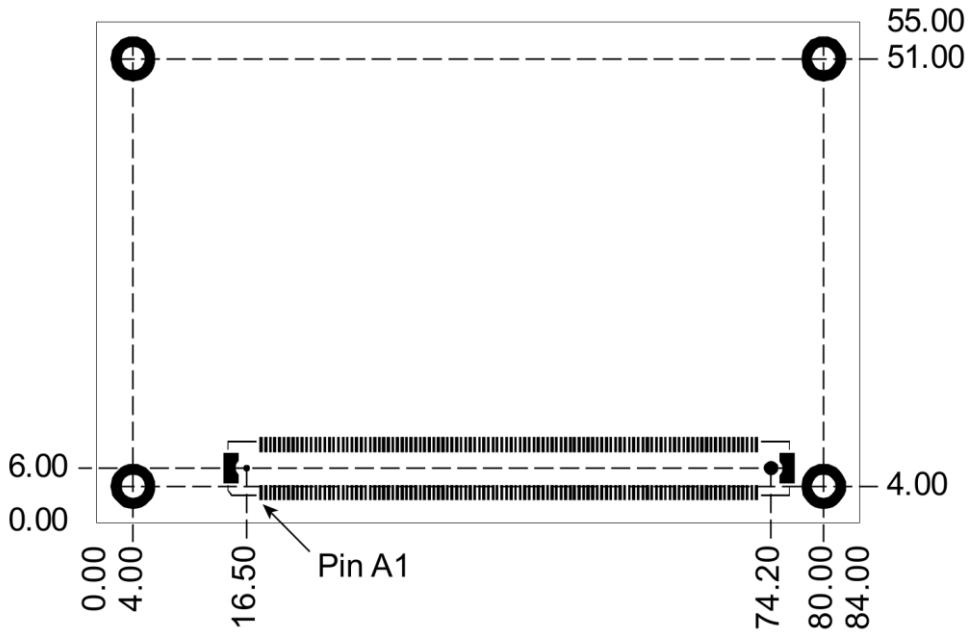
Warning:

Handle the COMe Module at electrostatic-free workstations only.

Do not handle or store the COMe Module near strong electrostatic, electromagnetic, magnetic or radioactive fields unless the COMe Module is contained within its original packaging.

1.6 MECHANICAL DEFINITIONS

Engicam COMe EHL has been designed respects the COMe Type 10 mechanical definitions. Figure below comes from PICMG® COM Express® Module Base Specification



CHAPTER 2

2. ORDERING INFORMATION

This Chapter gives the ordering information and technical specifications of the modules.

Section includes：

- **Ordering codes**
- **CPU & Memory specifications**
- **Operating temperature range**

2.1 ORDERING INFORMATION

Following are provided the ordering information and the description of the basic technical specifications for the modules:

Marking Code	Ordering Code	MPQ	Description	CPU & Memory specifications	Operating temperature range °C (excepted CPU)[2)]	Module available at least until [1)]
COMe EHL X6211E 32GB+8GB	0026800311E770	1	COMe Type 10, Intel X6211E dual core 6W,8GB LPDDR4,32GB **eMMC -25°C** [3)], LVDS, GB ethernet	Intel Atom X6212E dual core 6W 1.2 GHz, 1.5MB L2 cache, Industrial, -40 to +105 °C [2)] 32 bit LPDDR4 @4266MTs	-25 to +85	4thQ - 2031
COMe EHL X6211E 32GB+8GB	0026700311E770	58			-25 to +85	4thQ - 2031
COMe EHL X6211E 32GB+8GB	0026800314E770	1	COMe Type 10, Intel X6211E dual core 6W,8GB LPDDR4,32GB **eMMC -25°C** [3)], LVDS, GB ethernet	Intel Atom X6212E dual core 6W 1.2 GHz, 1.5MB L2 cache, Industrial, -40 to +105 °C [2)] 32 bit LPDDR4 @4266MTs	-25 to +85	4thQ - 2031
COMe EHL X6211E 32GB+8GB	0026700314E770	58			-25 to +85	4thQ - 2031
COMe EHL X6211E 32GB+8GB	0026800316E770	1	COMe Type 10, Intel X6211E dual core 6W,8GB LPDDR4,32GB **eMMC -25°C** [3)], LVDS, GB ethernet	Intel Atom X6212E dual core 6W 1.2 GHz, 1.5MB L2 cache, Industrial, -40 to +105 °C [2)] 32 bit LPDDR4 @4266MTs	-25 to +85	4thQ - 2031
COMe EHL X6211E 32GB+8GB	0026700316E770	58			-25 to +85	4thQ - 2031

[1)] **Long Term Availability based on INTEL longevity program**

[2)] ***Note: internal junction temperature (Temperature Range TJ Embedded SKUs: -40°C to 105°C - Industrial SKUs: -40°C to 110°C)***

[3)] ***Industrial eMMC option on request***

CHAPTER 3

3. PINOUT AND FEATURES

Section includes :

- Pinout overview
- COMe supported features

3.1 KEY FEATURES

SoC:

- Intel Atom X6211E Dual Core @ 1.2 GHz (burst 3.0 GHz) 1.5MB L2 cache, 6W
- Intel Atom X6413E Quad Core @ 1.5 GHz (burst 3.0 GHz) 1.5MB L2 cache, 9W
- Intel Atom X6425E Quad Core @ 1.8 GHz (burst 3.0 GHz) 1.5MB L2 cache, 12W)
- Intel Atom X6212RE Dual Core @ 1.2 GHz, 1.5MB L2 cache, 6W
- Intel Atom X6414RE Quad Core @ 1.5 GHz, 1.5MB L2 cache, 9W
- Intel Atom X6425RE Quad Core @ 1.9 GHz, 1.5MB L2 cache, 12W

Memory:

- Starting from 2GB LPDDR4-4266MTs on board

Storage:

- Starting from 4GB eMMC drive soldered on-board

Display & Graphics

- Intel® 11th generation (Gen 11) LP graphics controller
- DirectX 12.1 compliant, OpenGL ES 3.1/3.0/2.0/1.1, OpenGL 4.5 supported, OpenCL™ 1.2, Vulkan 1.0 APIs
- Dedicated FIVR for Graphics
- Intel® Virtualization Technology for Directed I/O (VT-d)
- eDP to LVDS Dual channel up to 1920x1080 @ 60Hz via eDP bridge;
- 1 x HDMI up to 4096x2160@60Hz
- 1x DP up to 4096x2160@60Hz
- eDP up to 4096x2160@60Hz

Audio

- HDA Interface

PCIe

- 6 x PCIe 3.0

Ethernet

- Gb Ethernet interface 2.5

I2C

- I2C

USB

- 2 x USB Host 3.0
- 8 x USB Host 2.0

LPC

- LPC interface

SATA

- 2 x SATA

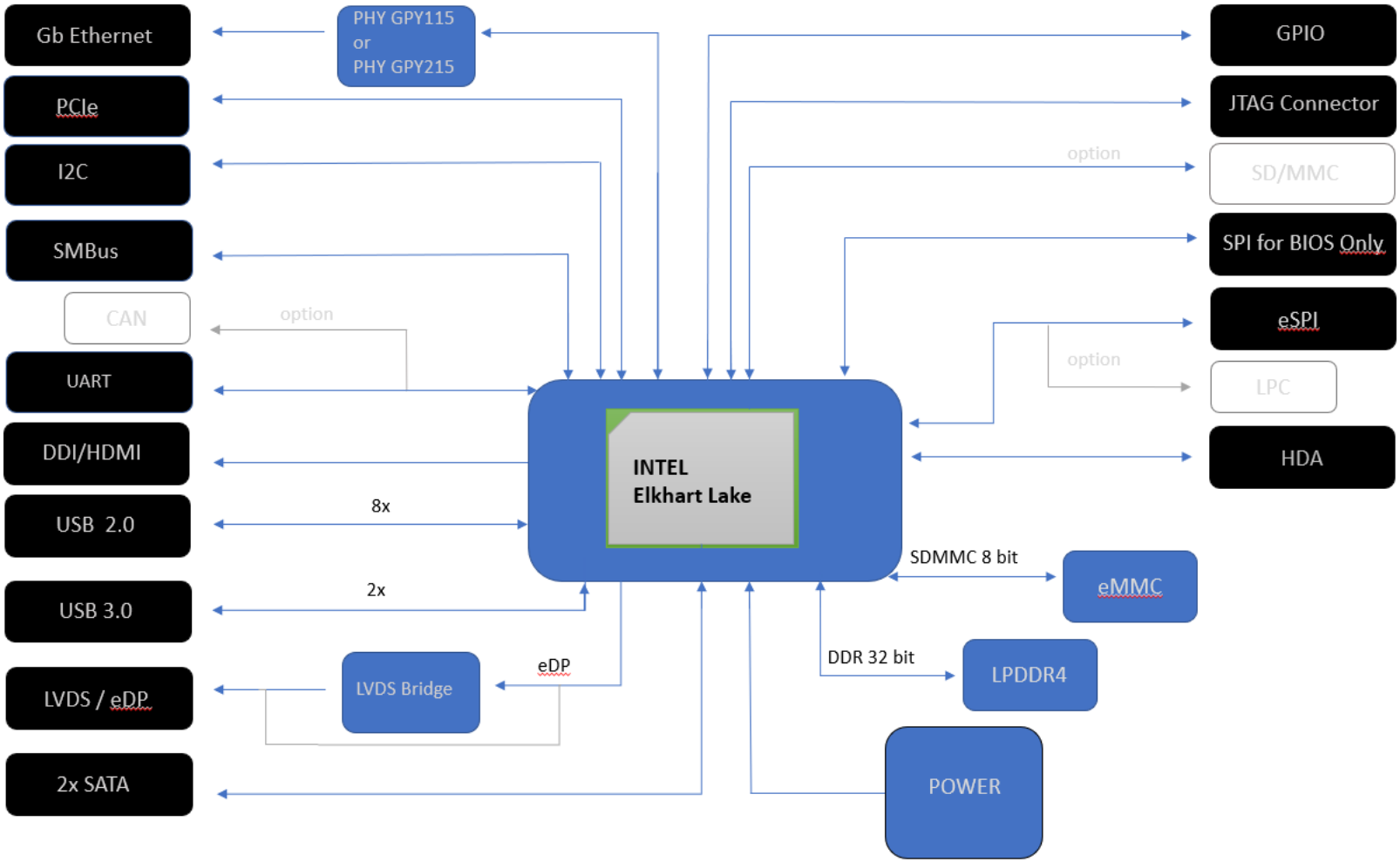
SPI

- ESPI interface
- SPI interface

DDI

- DDI interface

3.2 BLOCK DIAGRAM



3.3 MODULE PINOUT COMPARED WITH FULL SET COME

There are 314 edge fingers of the COMe module that mate with a low profile 314 pin 0.5mm pitch right angle connector. The following table lists the module pin assignments for all 314 edge fingers.

Row A	SIGNAL	GPIO	Row B	SIGNAL	GPIO
1	GND (FIXED)	-	1	GND (FIXED)	-
2	GBE0_MDI3-	N	2	GBE0_ACT#	N
3	GBE0_MDI3+	N	3	LPC_FRAME_N	Y
4	GBE0_nLINK100	N	4	LPC_AD0	Y
5	GBE0_nLINK1G	N	5	LPC_AD1	Y
6	GBE0_MDI2-	N	6	LPC_AD2	Y
7	GBE0_MDI2+	N	7	LPC_AD3	Y
8	GBE0_nLINK	N	8	LPC_DRQ0_N	Y
9	GBE0_MDI1-	N	9	LPC_DRQ1_N	Y
10	GBE0_MDI1+	N	10	LPC_CLK	Y
11	GND (FIXED)	-	11	GND (FIXED)	-
12	GBE0_MDI0-	-	12	COM_E_PWRBTN_N	Y
13	GBE0_MDI0+	N	13	SMB_CLK	Y
14	GBE0_CTREF	N	14	SMB_DATA	Y
15	PMC_SLP_S3_N_3V3	Y	15	SMB_ALLERTN	Y
16	SATA0_TXP	N	16	SATA1_TXP	N
17	SATA0_TXN	N	17	SATA1_TXN	N
18	PMC_SLP_S4_N_3V3	Y	18	SUS_STAT_N	-
19	SATA0_RXP	N	19	SATA1_RXP	N
20	SATA0_RXN	N	20	SATA1_RXN	N
21	GND (FIXED)	-	21	GND (FIXED)	-
22	USB3_0_RXN	N	22	USB3_0_TXN	N
23	USB3_0_RXP	N	23	USB3_0_TXP	N
24	SUS_SA5#	Y	24	COM_E_PWR_OK	-
25	USB3_1_RXN	N	25	USB3_1_TXN	N
26	USB3_1_RXP	N	26	USB3_1_TXP	N
27	COM_E_BATT_LOW_N	Y	27	WTD	Y
28	(S)ATA_ACT_N	Y	28	HDA_DIN2	-
29	HDA_SYNC	Y	29	HDA_DIN1	Y
30	HDA_RST_N	Y	30	HDA_DIN0	Y
31	GND (FIXED)	-	31	GND (FIXED)	-
32	HDA_BTCLK	Y	32	SPKR_STRP	Y
33	HDA_SDO	Y	33	PSE_I2C0_SCL	Y
34	BIOS_DIS0_N	-	34	PSE_I2C0_SDA	Y
35	H_PROCHOT_3V3_N	-	35	COM_E_THRM_N	-
36	USB2_6_DN	N	36	USB2_7_DN	N
37	USB2_6_DP	N	37	USB2_7_DP	N
38	USB_6_7_OC#	Y	38	USB_4_5_OC#	Y
39	USB2_4_DN	N	39	USB2_5_DN	N
40	USB2_4_DN	N	40	USB2_5_DP	N
41	GND (FIXED)	-	41	GND (FIXED)	-
42	USB2_2_DN	N	42	USB2_3_DN	N

43	USB2_2_DP	N	43	USB2_3_DP	N
44	USB_2_3_OC#	N	44	USB_0_1_OC#	Y
45	USB2_0_DP	N	45	USB2_1_DP	N
46	USB2_0_DP	N	46	USB2_1_DP	N
47	VCC_:RTC	-	47	+3V3A_DSW	Y
48	RSVD	-	48	USB0_HOST_PRSNT	N
49	GP_H03	Y	49	PMC_SYS_RESET_N	-
50	LPC_SERIRQ	Y	50	PMC_PLTRST_N_3V3	Y
51	GND (FIXED)	-	51	GND (FIXED)	-
52	PCIe_F_TXP	N	52	PCIe_F_RXP	N
53	PCIe_F_TXN	N	53	PCIe_F_RXN	N
54	GPIO	Y	54	GPO1	Y
55	PCIe_E_TXP	N	55	PCIe_E_TXP	N
56	PCIe_E_TXN	N	56	PCIe_E_TXN	N
57	GND	-	57	GPO2	Y
58	PCIe_D_TXP	N	58	PCIe_D_RXP	N
59	PCIe_D_TXN	N	59	PCIe_D_RXN	N
60	GND (FIXED)	-	60	GND (FIXED)	-
61	PCIe_C_TXP	N	61	PCIe_C_RXP	N
62	PCIe_C_TXN	N	62	PCIe_C_RXN	N
63	GPI1	Y	63	GPI3	Y
64	PCIe_B_TXP	N	64	PCIe_B_RXP	N
65	PCIe_B_TXN	N	65	PCIe_B_RXN	N
66	GND	-	66	PCIE_WAKE_N	Y
67	GPI2	Y	67	GEN_WAKE_N	Y
68	PCIe_A_TXP	N	68	PCIe_A_RXP	N
69	PCIe_A_TXN	N	69	PCIe_A_RXN	N
70	GND (FIXED)	-	70	GND (FIXED)	-
71	LVDS_A_P0_EDP_P2_TX_DP	N	71	DDI1_DP_TX0_DP	-
72	LVDS_A_P0_EDP_P2_TX_DN	N	72	DDI1_DP_TX0_DN	-
73	LVDS_A_P1_EDP_P2_TX_DP	N	73	DDI1_DP_TX1_DP	-
74	LVDS_A_P1_EDP_P2_TX_DN	N	74	DDI1_DP_TX1_DN	-
75	LVDS_A_P2_EDP_P2_TX_DP	N	75	DDI1_DP_TX2_DP	-
76	LVDS_A_P2_EDP_P2_TX_DN	N	76	DDI1_DP_TX2_DN	-
77	LVDS_VDD_EN	N	77	DDI0_PAIR4+	-
78	LVDS_A_P3_EDP_P2_TX_DP	N	78	DDI0_PAIR4-	-
79	LVDS_A_P3_EDP_P2_TX_DN	N	79	LVDS_BKLT_EN	N
80	GND (FIXED)	-	80	GND (FIXED)	-
81	LVDS_A_CK_EDP_P3_TX_DP	N	81	DDI1_DP_TX3_DP	-
82	LVDS_A_CK_EDP_P3_TX_DN	N	82	DDI1_DP_TX3_DN	-
83	LVDS_SCL_EDP_AUX_DN	N	83	LVDS_BKLT_CTRL	N
84	LVDS_SDA_EDP_AUX_DP	-	84	VCC_5V_SBY	-
85	GPI3	Y	85	VCC_5V_SBY	Y
86	RSVD	-	86	VCC_5V_SBY	-
87	EDP0_HPD	-	87	VCC_5V_SBY	-
88	PCIE_REF_CLK_REF+	N	88	BIOS_DIS1_N	-
89	PCIE_REF_CLK_REF-	N	89	DDI0_HPD	Y
90	GND (FIXED)	-	90	GND (FIXED)	-
91	+3V3A_1V8A_SPI	-	91	DDI0_PAIR5+	-
92	NFLASH_SPI0_MISO_E	-	92	DDI0_ PAIR5-	-
93	GPO0	Y	93	DDI0_ PAIR6+	-
94	NFLASH_SPI0_CLK_E	-	94	DDI0_ PAIR6-	-
95	NFLASH_SPI0_MOSI_E	-	95	DDI0_DDC_AUX_SEL	-
96	TPM_PP	-	96	USB7_HOST_PRSNT	-

97	TYPE10#	-	97	NFLASH_SPI0_CSN_E	-
98	UARTD_TXD/CAN0_TX	Y	98	DDI1_CTRLCLK_AUX_DP	-
99	UARTD_RXD/CAN0_RX	Y	99	DDI1_CTRLDATA_AUX_DN	-
100	GND (FIXED)	-	100	GND (FIXED)	-
101	UART1_TXD/CAN1_TX	Y	101	FAN_PWM15	-
102	UART1_RXD/CAN1_RX	Y	102	FAN_TACHIN	Y
103	INTRUDER_N	-	103	SLEEP_N	Y
104	VCC_12V	-	104	VCC_12V	-
105	VCC_12V	-	105	VCC_12V	-
106	VCC_12V	-	106	VCC_12V	-
107	VCC_12V	-	107	VCC_12V	-
108	VCC_12V	-	108	VCC_12V	-
109	VCC_12V	-	109	VCC_12V	-
110	GND (FIXED)	-	110	GND (FIXED)	-

Note:
The text in grey represents the signals defined in COMe specification, but not implemented in COMe EHL.

CHAPTER 4

4. POWER SUPPLY

Section includes :

- Power signals
- VDDIO Voltage Rail
- RTC battery
- Control signals and power sequences
- Boot modes
- Power states
- Watchdog

4.1 POWER SIGNALS

Read carefully the related sections before starting your power stage design. This module needs to be supplied up to +5Vin power. Refer to the table below for the power supply range specification.

Note: the system must provide at least a power of 3A at 12V to allow the start of the module.

	Min	Typ	Max
Voltage range	+5V	+12V	+20V
Module Current @ 12V	-	TBD mA	-

Note: *the measures in the table above are to be considered referred to the module with only the OS running, the use of graphics accelerators or other multimedia applications could be the cause of higher consumption than those indicated.*

The following table shows the module power supply pins numbering. It's strongly recommended to connect all power supply pins in order to avoid damage.

ROW A-Pin	Name	Primary Function Description	ROW B-Pin	Name	Primary Function Description
1	GND	Power return-Ground reference	1	GND	Power return-Ground reference
11	GND	Power return-Ground reference	11	GND	Power return-Ground reference
21	GND	Power return-Ground reference	21	GND	Power return-Ground reference
31	GND	Power return-Ground reference	31	GND	Power return-Ground reference
41	GND	Power return-Ground reference	41	GND	Power return-Ground reference
51	GND	Power return-Ground reference	51	GND	Power return-Ground reference
57	GND	Power return-Ground reference	60	GND	Power return-Ground reference
60	GND	Power return-Ground reference	70	GND	Power return-Ground reference
66	GND	Power return-Ground reference	80	GND	Power return-Ground reference
70	GND	Power return-Ground reference	90	GND	Power return-Ground reference
80	GND	Power return-Ground reference	100	GND	Power return-Ground reference
90	GND	Power return-Ground reference	110	GND	Power return-Ground reference
100	GND	Power return-Ground reference			
110	GND	Power return-Ground reference			
104	VCC_12V	Power input voltage 12V	104	VCC_12V	Power input voltage 12V
105	VCC_12V	Power input voltage 12V	105	VCC_12V	Power input voltage 12V
106	VCC_12V	Power input voltage 12V	106	VCC_12V	Power input voltage 12V
107	VCC_12V	Power input voltage 12V	107	VCC_12V	Power input voltage 12V
108	VCC_12V	Power input voltage 12V	108	VCC_12V	Power input voltage 12V
109	VCC_12V	Power input voltage 12V	109	VCC_12V	Power input voltage 12V

4.2 VDDIO VOLTAGE RAIL

The module is compliant to COMe_Specification_V3.

For details referred to COMe_Specification_V3 chapter 7 table 7.1-7.2 input power of this document.

4.3 RTC BATTERY

The standard provides a signal to power supply a RTC on module. If not used this pin may be left floating.

Pin	Name	Type / Tolerance	Use
A47	VDD_RTC	Power In	Low current RTC circuit backup power – 3.3V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.
		Power Out (when charging a Super Cap)	The connection with module is obtained by connecting directly the backup battery to the VDD_RTC signal. **Note:** *The module is already designed to manage the charge of backup battery, by a siple 1KOhm series resistor from 3.1V.*

The consumption to feed the RTC when the module is powered off is about 6uA (to be confirmed) at the nominal battery voltage (3.3 V)

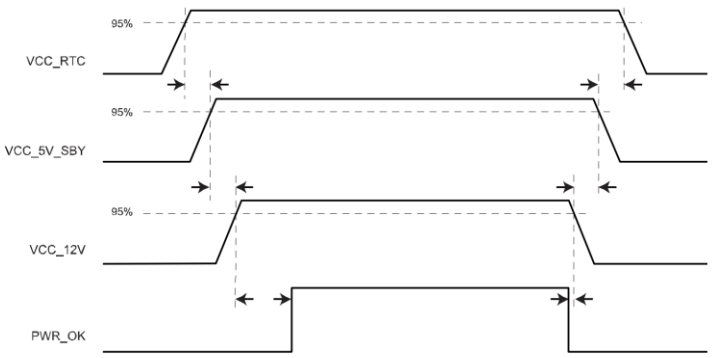
4.4 CONTROL SIGNALS AND POWER SEQUENCES

4.4.1 STANDARD POWER SEQUENCES

COM Express input power sequencing requirements are as follows:

VCC_RTC ***shall*** come up at the same time or before VCC_5V_SBY comes up
VCC_5V_SBY ***shall*** come up at the same time or before VCC_12V comes up
PWR_OK ***shall*** be active at the same time or after VCC_12V comes up
PWR_OK ***shall*** be inactive at the same time or before VCC_12V goes down
VCC_12V ***shall*** go down at the same time or before VCC_5V_SBY goes down
VCC_5V_SBY ***shall*** go down at the same time or before VCC_RTC goes down

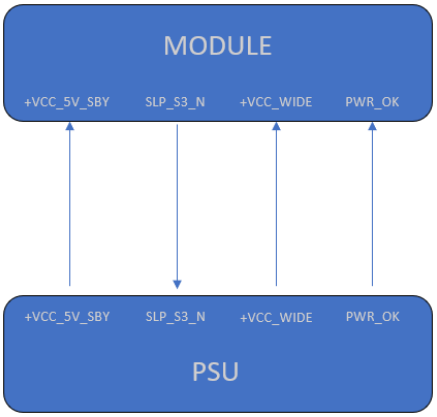
Figure 7-1: Power Sequencing



4.4.2 POWER SEQUENCES COME TYPE10 EHL

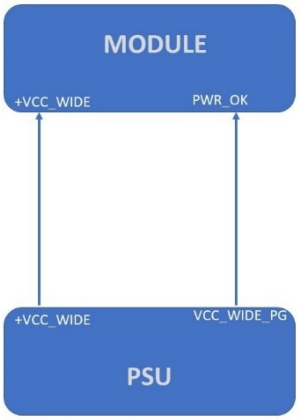
It is possible to supply the module either from the VCC_5V_SBY or VCC_WIDE signal.

Using the VCC_5V_SBY:



PSU transfers 5V_SBY to the module; the module puts the system into Soft-Off Status and provides VCC_WIDE_EN signal to the supply unit. The PSU generates the VCC_WIDE rail and finally the PWR_OK signal, which indicates to the CPU that the power rail is stable.

Using VCC_WIDE



The PSU generates the VCC_WIDE rail and finally the PWR_OK signal, which indicates to the CPU that the power rail is stable.

NAME	TYPICAL INPUT RANGE
VCC_5V_SBY	4.75 – 5.25 V
VCC_WIDE	11.4 – 12.6 V

4.4.3 ABSOLUTE VALUES

Absolute values must never be passed.

NAME	ABSOLUTE INPUT RANGE
VCC_5V_SBY	4.6 – 5.5 V
VCC_WIDE	4.6 - 22 V

4.4.4 CONTROL SIGNALS

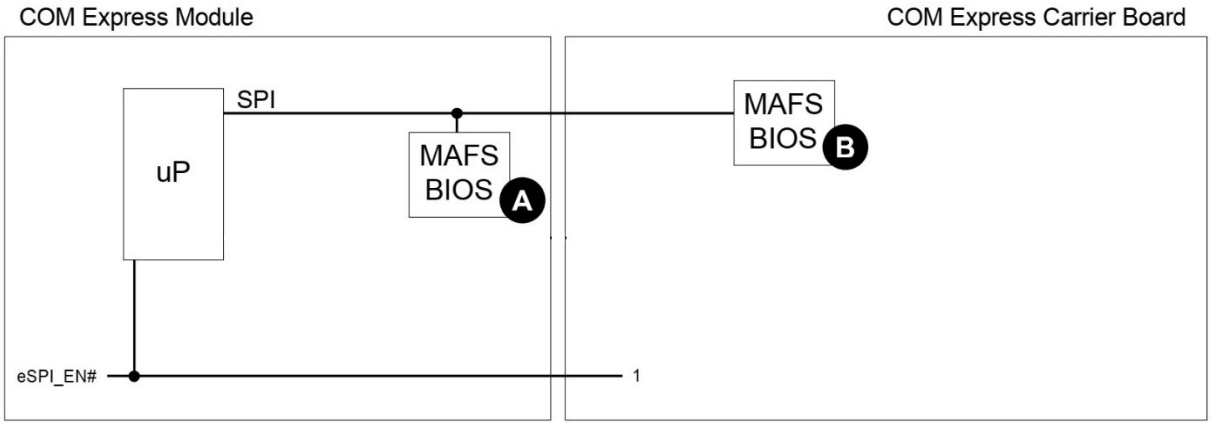
PIN	NAME	CPU PIN NAME	DIRECTION	RAIL	Function Description
B12	PWRBTN#	GP_DSW03_PMC_PWRBTN_N	IN	+3.3V	A falling edge creates a power button event
B49	SYS_RESET#	PMC_SYS_RESET_N	IN	+3.3V	Reset button input. Active low request for Module to reset and reboot
B50	CB_RESET#	GP_B13_PMC_PLTRST_N	OUT	+3.3V	Reset output from Module
B24	PWR_OK	VCCIO_PG	IN	+3.3V	Power OK from main power supply.
B18	SUS_STAT#	SUS_STAT#	OUT	+3.3V	Indicates imminent suspend operation; used to notify LPC devices.
A15	SUS_S3#	GP_DSW04_PMC_SLP_S3_N	OUT	+3.3V	Indicates system is in Suspend to RAM state.
A18	SUS_S4#	GP_DSW05_PMC_SLP_S4_N	OUT	+3.3V	Indicates system is in Suspend to Disk state.
A24	SUS_S5#	GP_DSW10_PMC_SLP_S5_N	OUT	+3.3V	Indicates system is in Soft Off state.
B66	WAKE0#	PCIE_WAKE_N	IN	+3.3V	PCI Express wake up signal.
B67	WAKE1#	GEN_WAKE_N	IN	+3.3V	General purpose wake up signal.
A27	BATLOW#	GP_DSW00_PMC_BATLOW_N	IN	+3.3V	Indicates that external battery is low.
A103	LID#	INTRUDER_N	IN	+3.3V/+12V	LID switch
B103	SLEEP#	GP_T10_PSE_HSUART2_RE	IN	+3.3V/+12V	Sleep button
A35	THRMTRIP#	THRMTRIP#	OUT	+3.3V	Active low output indicating that the CPU has entered thermal shutdown.
A47	VCC_:RTC	RTC_RST_N		-	Real-time clock circuit-power input.
B27	WTD	GP_B11_PMC_ALERT_N_PSE_TGPIO06	OUT	+3.3V	Output indicating that a watchdog time-out event has occurred.
B35	THRM#	THRM#	IN	+3.3V	Input from off-Module temp sensor indicating an over-temp situation.
A34	BIOS_DIS0#/ESPI_SAFS	BIOS_DIS0#/ESPI_SAFS	IN	-	Selection strap to determine the BIOS boot device.
B88	BIOS_DIS1#	BIOS_DIS1#	IN	-	Selection strap to determine the BIOS boot device.

4.5 BOOT MODE

UEFI EDK2 can be configured via Slim Bootloader upon request.

4.5.1 SPI BOOT FLASH

Master Attached Flash Sharing (MAFS) is defined as the BIOS Flash directly attached to the processor SPI bus. The operating mode is described in the following figure.



*** figure from COM Express Module Base Specification**

The module can direct the chipset's chip select to internal flash Memory or external flash memory. The chip select drive is defined by the BIOS_DIS1# (pin B88) and BIOS_DIS0# (pin A34) signals.

BIOS_DIS0	BIOS_DIS1	Function
Open	Open	Boot on internal flash
GND	Open	Boot on internal flash
Open	GND	Not used
GND	GND	Boot on external flash

4.6 POWER STATES

The Advanced Configuration and Power Interface (ACPI) 4.0 enables the system to power down and save power when not required (suspend) and wake up when required (resume).

STATUS	Module Status	Carrier Status	Status Description
Soft-Off			System is off, but the carrier board input supply is available
Suspend-to-disk / Hibernate	The module is in the standby mode all the features are off except the wakeup capable one	All the power rails are available, while the peripherals are stopped via software	System is suspended and waits for a wakeup source (TBT).
Wake-up-event state	CPU is available at 100%	All power rails are on and all the peripherals and CPU features are available	System is running

CHAPTER 5

5. INTERFACES

Section includes :

- HDA
- GB Ethernet
- SATA
- PCIe
- USB 3.0
- USB 2.0
- LVDS
- ESPI/LPC
- SPI
- DDI
- SERIAL
- SM Bus
- I2C Bus
- Miscellaneous
- UART
- CAN

5.1 HIGH DEFINITION AUDIO

High Definiton Audio is an audio standard developed by Intel. It is superior digital audio on the PC for an immersive surround-sound experience, high-quality speech recognition and Voice over IP capabilities, as well as enabling Dolby audio enjoyment of PCs.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
A30	HDA_RST#	GP_R04/HDA_RST_N/DMIC_CLK_A1	Reset output to CODEC, active low	O-CMOS	3V3
A29	HDA_SYNC	GP_R01/HDA_SYNC/AVS_I2S0_SFRM/PSE_I2S0_SFRM	Sample-synchronization signal to the CODEC(s).	O-CMOS	3V3
A32	HDA_BITCLK	GP_R00/HDA_BCLK/AVS_I2S0_SCLK/PSE_I2S0_SCLK	Serial data clock generated by the external CODEC(s).	I/O-CMOS	3V3
A33	HDA_SDOUT	GP_R02/HDA_SDO/AVS_I2S0_TXD/PSE_I2S0_TXD/DMIC_CLK_B0	Serial TDM data output to the CODEC.	O-CMOS	3V3
B30	HDA_SDIN0	GP_R03/HDA_SDI0/AVS_I2S0_RXD/PSE_I2S0_RXD/DMIC_CLK_B1	Serial TDM data inputs	I/O-CMOS	3V3
B29	HDA_SDIN1	GP_R05/HDA_SDI1/AVS_I2S1_RXD/DMIC_DATA1	Serial TDM data inputs	I/O-CMOS	3V3

5.2 GB ETHERNET

One Gigabit Ethernet port is defined, designated GBE0. The ports may operate in 10, 100, 1000 or 2500 Mbit/sec modes. It's possible to mount PHY GPY115 or PHY GPY215.

PIN	NAME	PHY PIN NAME	Description	TYPE	RAIL
A2	GBE0_MDI3-	TPIDP	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3.	Analog	3.3V
A3	GBE0_MDI3+	TPIDN	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3.	I/O	3.3V
A4	GBE0_LINK100#	GPHY_LED0	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	OD CMOS	3.3V
A5	GBE0_LINK1000#	GPHY_LED2	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low	OD CMOS	3.3V
A6	GBE0_MDI2-	TPICP	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3.	Analog	3.3V
A7	GBE0_MDI2+	TPICN	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3.	I/O	3.3V
A8	GBE0_LINK#	GPHY_LED1	Gigabit Ethernet Controller 0 link indicator, active low	OD CMOS	3.3V
A9	GBE0_MDI1-	TPIBP	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3.	Analog	3.3V
A10	GBE0_MDI1+	TPIBN	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3.	I/O	3.3V
A12	GBE0_MDI0-	TPIAP	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3.	Analog	3.3V
A13	GBE0_MDI0+	TPIAN	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3.	I/O	3.3V
A14	GBE0_CTREF	-	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.	REF	GND min 3.3V max
B2	GBE0_ACT#	GPHY_LED3	OD CMOS	OD CMOS	3.3V

5.3 SATA

Serial ATA links for support of existing SATA-150 and SATA-600 devices.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
A16	SATA0_TX+	PCIE_8_TXP/SATA_0_TXP/GBE_SGMII_TXP	Serial ATA Channel 0 transmit differential pair	O-STATA	AC coupled on Module
A17	SATA0_TX-	PCIE_8_TXN/SATA_0_TXN/GBE_SGMII_TXN			
A19	SATA0_RX+	PCIE_8_RXP/SATA_0_RXP/GBE_SGMII_RXP	Serial ATA Channel 0 receive differential pair	I-STATA	AC coupled on Module
A20	SATA0_RX-	PCIE_8_RXN/SATA_0_RXN/GBE_SGMII_RXN			
B16	SATA1_TX+	PCIE_9_TXP/SATA_1_TXP/PSE_GBE1_SGMII_TXP	Serial ATA Channel 1 transmit differential pair	O-STATA	AC coupled on Module
B17	SATA1_TX-	PCIE_9_TXN/SATA_1_TXN/PSE_GBE1_SGMII_TXN			
B19	SATA1_RX+	PCIE_9_RXP/SATA_1_RXP/PSE_GBE1_SGMII_RXP	Serial ATA Channel 1 receive differential pair	I-STATA	AC coupled on Module
B20	SATA1_RX-	PCIE_9_RXN/SATA_1_RXN/PSE_GBE1_SGMII_RXN			
A28	(S)ATA_ACT#	GP_E00/SATA_LED_N/SATAXPCIE_0/SATA_0_GP	Serial ATA (activity indicator, active low	I/O-CMOS	3V3

5.4 PCIE

Peripheral Component Interface Express – next-generation high speed Serialized I/O bus. Compliant with the specification the module implements the PCIe Link A port.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
A68	PCIE_TX0+	PCIE_0_TXP/USB3_2_TXP	PCI Express Differential Transmit Pairs	O-PCIE	AC coupled on Module
A69	PCIE_TX0-	PCIE_0_TXN/USB3_2_TXN			
B68	PCIE_RX0+	PCIE_0_RXP/USB3_2_RXP	PCI Express Differential Receive Pairs	I-PCIE	AC coupled on Module
B69	PCIE_RX0-	PCIE_0_RXN/USB3_2_RXN			
A64	PCIE_TX1+	PCIE_1_TXP/USB3_3_TXP	PCI Express Differential Transmit Pairs	O-PCIE	AC coupled on Module
A65	PCIE_TX1-	PCIE_1_TXN/USB3_3_TXN			
B64	PCIE_RX1+	PCIE_1_RXP/USB3_3_RXP	PCI Express Differential Receive Pairs	I-PCIE	AC coupled on Module
B65	PCIE_RX1-	PCIE_1_RXN/USB3_3_RXN			
A61	PCIE_TX2+	PCIE_2_TXP	PCI Express Differential Transmit Pairs	O-PCIE	AC coupled on Module
A62	PCIE_TX2-	PCIE_2_TXN			
B61	PCIE_RX2+	PCIE_2_RXP	PCI Express Differential Receive Pairs	I-PCIE	AC coupled on Module
B62	PCIE_RX2-	PCIE_2_RXN			
A58	PCIE_TX3+	PCIE_3_TXP	PCI Express Differential Transmit Pairs	O-PCIE	AC coupled on Module
A59	PCIE_TX3-	PCIE_3_TXN			
B58	PCIE_RX3+	PCIE_3_RXP	PCI Express Differential Receive Pairs	I-PCIE	AC coupled on Module
B59	PCIE_RX3-	PCIE_3_RXN			
A55	PCIE_TX4+	PCIE_6_TXP/UFS_1_TXP0/GBE_SGMII_TXP	PCI Express Differential Transmit Pairs	O-PCIE	AC coupled on Module
A56	PCIE_TX4-	PCIE_6_TXN/UFS_1_TXN0/GBE_SGMII_TXN			
B55	PCIE_RX4+	PCIE_6_RXP/UFS_1_RXP0/GBE_SGMII_RXP	PCI Express Differential Receive Pairs	I-PCIE	AC coupled on Module
B56	PCIE_RX4-	PCIE_6_RXN/UFS_1_RXN0/GBE_SGMII_RXN			
A52	PCIE_TX5+	PCIE_7_TXP/UFS_1_TXP1/PSE_GBE1_SGMII_TXP	PCI Express Differential Transmit Pairs	O-PCIE	AC coupled on Module
A53	PCIE_TX5-	PCIE_7_TXN/UFS_1_TXN1/PSE_GBE1_SGMII_TXN			
B52	PCIE_RX5+	PCIE_7_RXP/UFS_1_RXP1/PSE_GBE1_SGMII_RXP	PCI Express Differential Receive Pairs	I-PCIE	AC coupled on Module
B53	PCIE_RX5-	PCIE_7_RXN/UFS_1_RXN1/PSE_GBE1_SGMII_RXN			
A88	PCIe_REF_CLK+	PCIE_CLK0_DP	Reference clock output for all PCI Express	O-PCIE	PCIE
A89	PCIe_REF_CLK-	PCIE_CLK2_DN			

5.5 USB3.0

USB 3.0 is the third major version of the Universal Serial Bus (USB) standard for interfacing computers and electronic devices that can transfer data at up to 5 Gbit/s.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
B22	USB_SSTX0-	USB3_0_TXN	USB 3.1 Differential Transmit Pair 1	O-USB	USB
B23	USB_SSTX0+	USB3_0_TXP	USB 3.1 Differential Transmit Pair 1	O-USB	USB
A22	USB_SSRX0-	USB3_0_RXN	USB 3.1 Differential Receive Pair 1	I-USB	USB
A23	USB_SSRX0+	USB3_0_RXP	USB 3.1 Differential Receive Pair 1	I-USB	USB
B25	USB_SSTX1-	USB3_1_TXN	USB 3.1 Differential Transmit Pair 2	O-USB	USB
B26	USB_SSTX1+	USB3_1_TXP	USB 3.1 Differential Transmit Pair 2	O-USB	USB
A25	USB_SSRX1-	USB3_1_RXN	USB 3.1 Differential Receive Pair 2	I-USB	USB
A26	USB_SSRX1+	USB3_1_RXP	USB 3.1 Differential Receive Pair 2	I-USB	USB

5.6 USB 2.0

The USB0 port is available as a USB 2.0.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
A46	USB0+	USB2_0_DP	USB 2.0 Port 1 Transmit Differential	I-USB	USB
A45	USB0-	USB2_0_DN	USB 2.0 Port 1 Receive Differential	O-USB	USB
B46	USB1+	USB2_1_DP	USB 2.0 Port 2 Transmit Differential	I-USB	USB
B45	USB1-	USB2_1_DN	USB 2.0 Port 2 Receive Differential	O-USB	USB
A43	USB2+	USB2_2_DP	USB 2.0 Port 3 Transmit Differential	I-USB	USB
A42	USB2-	USB2_2_DN	USB 2.0 Port 3 Receive Differential	O-USB	USB
B43	USB3+	USB2_3_DP	USB 2.0 Port 4 Transmit Differential	I-USB	USB
B42	USB3-	USB2_3_DN	USB 2.0 Port 4 Receive Differential	O-USB	USB
A40	USB4+	USB2_4_DP	USB 2.0 Port 5 Transmit Differential	I-USB	USB
A39	USB4-	USB2_4_DN	USB 2.0 Port 5 Receive Differential	O-USB	USB
B40	USB5+	USB2_5_DP	USB 2.0 Port 6 Transmit Differential	I-USB	USB
B39	USB5-	USB2_5_DN	USB 2.0 Port 6 Receive Differential	O-USB	USB
A37	USB6+	USB2_6_DP	USB 2.0 Port 7 Transmit Differential	I-USB	USB
A36	USB6-	USB2_6_DN	USB 2.0 Port 7 Receive Differential	O-USB	USB
B37	USB7+	USB2_7_DP	USB 2.0 Port 8 Transmit Differential	I-USB	USB
B36	USB7-	USB2_7_DN	USB 2.0 Port 8 Receive Differential	O-USB	USB

5.7 LOW VOLTAGE DIFFERENTIAL SIGNALING

The LVDS lines are high-speed signals; to avoid disturbances and reduce noise on the line we suggest routing the channel lines in differential mode. For the same reason also the “channel” on the cable used to connect the board to TFT should be twisted. An eDP to LVDS bridge is present.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
A71	LVDS_A0+	DDI0_TXP0	LVDS Channel A differential pairs	O-LVDS	LVDS
A72	LVDS_A0-	DDI0_TXN0		O-LVDS	LVDS
A73	LVDS_A1+	DDI0_TXP1	LVDS Channel A differential pairs	O-LVDS	LVDS
A74	LVDS_A1-	DDI0_TXN1		O-LVDS	LVDS
A75	LVDS_A2+	DDI0_TXP2	LVDS Channel A differential pairs	O-LVDS	LVDS
A76	LVDS_A2-	DDI0_TXN2		O-LVDS	LVDS
A77	LVDS_VDD_EN	PNL0_VDDEN	LVDS panel power enable	O-CMOS	3.3V
A78	LVDS_A3+	DDI0_TXP3	LVDS Channel A differential pairs	O-LVDS	LVDS
A79	LVDS_A3-	DDI0_TXN3		O-LVDS	LVDS
A81	LVDS_A_CK+	DDI0_TXP3	LVDS Channel B differential clock	O-LVDS	LVDS
A82	LVDS_A_CK-	DDI0_TXN3		O-LVDS	LVDS
A83	LVDS_I2C_CK	DDI0_AUXN	I2C clock output for LVDS display use	I/O-OD-CMOS	3.3V
A84	LVDS_I2C_DAT	DDI0_AUXP		I/O-OD-CMOS	3.3V
B79	LVDS_BKLT_EN	PNL0_BKLTEN	LVDS panel backlight enable	O-CMOS	3.3V
B83	LVDS_BKLT_CTRL	PNL0_BKLTCTL	LVDS panel backlight brightness control	O-CMOS	3.3V

5.8 ESPI/LPC

5.8.1 ESPI

The Module LPC and eSPI interface share connector pins. A Module design may support either LPC or eSPI.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
B3	ESPI_CS0#	GP_G20/ ESPI_CSO_N	eSPI chip select	I/O CMOS	3.3V
B4	ESPI_IO_0	GP_G15/ ESPI_IO0	Bi-directional data signals used to transfer data between PCH and eSPI slave device	I/O CMOS	3.3V
B5	ESPI_IO_1	GP G16/ ESPI_IO1	Bi-directional data signals used to transfer data between PCH and eSPI slave device	I/O CMOS	3.3V
B6	ESPI_IO_2	GP_G17/ ESPI_IO2/ PMC_SUSPWRDNACK	Bi-directional data signals used to transfer data between PCH and eSPI slave device	I/O CMOS	3.3V
B7	ESPI_IO_3	GP_G18/ ESPI_IO3/ PMC_SUSACK_N	Bi-directional data signals used to transfer data between PCH and eSPI slave device	I/O CMOS	3.3V
B8	ESPI_ALERT0#	GP_B03/ CPU_GP2/ ESPI_ALERT0_N/ PSE_TGPIO26	eSPI alert signal	I CMOS	3.3V
B9	ESPI_ALERT1#	GP_B04/ CPU_GP3/ ESPI_ALERT1_N/ PSE_TGPIO27	eSPI alert signal	I CMOS	3.3V
B10	ESPI_CLK	GP_G21/ ESPI_CLK	eSPI Clock output from PCH	O CMOS	3.3V
B18	ESPI_RESET#	-	eSPI Reset Reset the eSPI interface for both master and slaves	O CMOS	NA
B47	ESPI_EN#	-	LPC/eSPI mode selection	I CMOS	NA
A34	ESPI_SAFS	-	Serial Interrupt Request	I/OD-3.3	3.3V
A50	ESPI_CS1#	GP_B15/SIO_SPI0_CS0_N/PSE_SPI2_CS0_N / ESPI_CS1_N	BIOS Selection Strap 0	I CMOS	3.3V

5.8.2 LPC (OPTIONAL)

Low Pin-Count Interface is a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
B3	LPC_FRAME#	-	LPC Frame Indicator	O CMOS	3.3V
B4	LPC_AD0	-	LPC Multiplexed Command, Address & Data 0	I/O CMOS	3.3V
B5	LPC_AD1	-	LPC Multiplexed Command, Address & Data 1	I/O CMOS	3.3V
B6	LPC_AD2	-	LPC Multiplexed Command, Address & Data 2	I/O CMOS	3.3V
B7	LPC_AD3	-	LPC Multiplexed Command, Address & Data 3	I/O CMOS	3.3V
B8	LPC_DRQ0#	-	LPC Serial DMA/Master Request 0	I CMOS	3.3V
B9	LPC_DRQ1#	-	LPC Serial DMA/Master Request 1	I CMOS	3.3V
B10	LPC_CLK	-	24MHz LPC clock	O CMOS	3.3V
B47	ESPI_EN#	-	LPC/eSPI mode selection	I CMOS	NA
A34	LPC_SERIRQ	-	Serial Interrupt Request	I/OD-3.3	3.3V

5.9 SERIAL PERIPHERAL INTERFACE

The following tables describe the Enhanced Configurable SPI signals.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
A91	SPI_POWER	-	SPI_POWER 3.3V Power Output Pin for external SPI flash	O CMOS	3.3V
A92	SPI_MISO	FSPI_MISO_IO1	SPI_MISO SPI Master IN Slave OUT I-3.3	I CMOS	3.3V
A94	SPI_CLK	FSPI_CLK	SPI_CLK SPI Clock O-3.3 0 R	O CMOS	3.3V
A95	SPI_MOSI	FSPI_MOSI_IO0	SPI_MOSI SPI Master Out Slave In	I CMOS	3.3V
B97	SPI_CS#	FSPI_CS1_N	SPI_CS# SPI Chip Select	O CMOS	3.3V

5.10 DIGITAL DISPLAY INTERFACES

Digital Display Interfaces (DDI) provide DisplayPort and HDMI/DVI interfaces. Type 10 Modules use DDI to provide DisplayPort and HDMI/DVI interfaces; can contain a single DDI (DDI[0]) that can support DisplayPort and HDMI/DVI.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
B71	DDI0_PAIR0+	DDI1_TXP0	DDI 0 Pair differential pairs	O PCIE	AC coupled off Module
B72	DDI0_PAIR0-	DDI1_TXN0	DDI 0 Pair differential pairs	O PCIE	AC coupled off Module
B73	DDI0_PAIR1+	DDI1_TXP1	DDI 0 Pair differential pairs	O PCIE	AC coupled off Module
B74	DDI0_PAIR1-	DDI1_TXN1	DDI 0 Pair differential pairs	O PCIE	AC coupled off Module
B75	DDI0_PAIR2+	DDI1_TXP2	DDI 0 Pair differential pairs	O PCIE	AC coupled off Module
B76	DDI0_PAIR2-	DDI1_TXN2	DDI 0 Pair differential pairs	O PCIE	AC coupled off Module
B81	DDI0_PAIR3+	DDI1_TXP3	DDI 0 Pair differential pairs	O PCIE	AC coupled off Module
B82	DDI0_PAIR3-	DDI1_TXN3	DDI 0 Pair differential pairs	O PCIE	AC coupled off Module
B89	DDI0_HPD	GP_E03/ DDI1_HPD/ PNL_MISC_DDI1_CPU/ GP0_PSE_TGPIO15	DDI Hot-Plug Detect	I CMOS	3.3V
B95	DDI0_DDC_AUX_SEL	GPU_UI17_ISI_OKNOK_1	This pin shall have a 1M pull-down to logic ground on the Module.	I CMOS	AC coupled off Module
B98	DDI0_CTRLCLK_AUX+	DDI1_AUXP	DP AUX+ function if DDI[0]_DDC_AUX_SEL is no connect	I/O PCIE	AC coupled off Module
			HDMI/DVI I2C CTRLCLK if DDI[0]_DDC_AUX_SEL is pulled high	I/O OD CMOS	3.3V
B99	DD 0_CTRLDATA_AUX-	DDI1_AUXN	DP AUX- function if DDI[0]_DDC_AUX_SEL is no connect	I/O PCIE	AC coupled off Module
			HDMI/DVI I2C CTRLDATA if DDI[0]_DDC_AUX_SEL is pulled high	I/O OD CMOS	3.3V

5.11 GENERAL PURPOSE SERIAL INTERFACE

General Purpose Serial Interface is a 7 wire communications interface. It is used as an interface between Ethernet MAC and PHY blocks.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
A98	SER0_TX	GP_E15/ PSE_I2S0_RXD/ PSE_CAN0_TX/ PSE_TGPIO17	General purpose serial port transmitter. This pin is shared with CAN_TX	O CMOS-T	3.3V/12V
A99	SER0_RX	GP_E16/ PSE_I2S0_RXD/ PSE_CAN0_TX/ PSE_TGPIO16	General purpose serial port receiver. This pin is shared with CAN_RX	I CMOS-T	3.3V/12V
A101	SER1_TX	GP_E20/ PSE_I2S0_RXD/ PSE_CAN0_TX/ PSE_TGPIO14	General purpose serial port transmitter. This pin is shared with CAN_TX	O CMOS-T	3.3V/12V
A102	SER1_RX	GP_E21/ PSE_I2S0_RXD/ PSE_CAN0_TX/ PSE_TGPIO15	General purpose serial port receiver. This pin is shared with CAN_RX	I CMOS-T	3.3V/12V

5.12 SMBUS

The SMBus port is specified for system management functions. It is used on the Module to manage system functions such as reading the DRAM SPD EEPROM and setting clock synthesizer parameters.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
B13	SMB_CK	GP_C00/ SMB_CLK/ PSE_I2C3_SCL/ PSE_TGPIO18	System Management Bus bidirectional clock line.	I/O OD CMOS	3.3V Suspend/ 3.3V
B14	SMB_DAT	GP_C01/ SMB_DATA/ PSE_I2C3_SCL/ PSE_TGPIO19	System Management Bus bidirectional data line.	I/O OD CMOS	3.3V Suspend/ 3.3V
B15	SMB_ALLERT#	GP_C02/ PSE_PWMO0/ SMB_ALERT_N/ PSE_TGPIO29	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I/O OD CMOS	3.3V Suspend/ 3.3V

5.13 I2C BUS

The I2C port shall be available in addition to the SMBus.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
B33	I2C_CK	GP_B05/ PSE_I2C0_SCL/ PSE_TGPIO06	General purpose I2C port clock output	I/O OD CMOS	3.3V Suspend/ 3.3V
B34	I2C_DAT	GP_B06/ PSE_I2C0_SCL/ PSE_TGPIO07	General purpose I2C port data I/O line	I/O OD CMOS	3.3V Suspend/ 3.3V

5.14 MISCELLANEOUS

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
B32	SPKR	GP_B14/ SPKR_PMC/ TGPIO1_SIO_SPI0_CSI_N/ PSE_SPI2_CSI_N	Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.	O CMOS	3.3V
B101	FAN_PWMOUT	GP_H11/ PCIE_CLK_REQ5_N/ PSE_PWM15	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O OD CMOS	3.3V / 12V
B102	FAN_TACHIN	GP_T03/ SIO_I2C7_SCL/ PSE_TGPIO06	Fan tachometer input for a fan with a two pulse output	I OD CMOS	3.3V / 12V
A96	TPM_PP	PP (on TPM 2.0)	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I CMOS	3.3V

5.15 UART (OPTION)

The COMe Type 10 module does not include UARTs, but they can be optional.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
A101	UART0_TXD [1)]	GP_C13/ PSE_UART0_TXD/ SIO_YART1_TXD	UART0 TXD signal	Y	+3,3V
A102	UART0_RXD [1)]	GP_C12/ PSE_UART0_RXD/ SIO_UART1_RXD	UART0 RTS signal	Y	+3,3V
A54	UART1_TXD	GP_H13/ PSE_UART1_TXD/ M2_SKT2_CFG1/ PSE_TGPIO52	UART1 TXD signal	Y	+3,3V
A63	UART1_RXD	GP_H12/ PSE_UART1_RXD/ M2_SKT2_CFG0/ PSE_TGPIO51	UART1 RTS signal	Y	+3,3V
A67	UART3_TXD	GP_C17/ GBE_MDC/ PSE_UART3_TXD/ SIO_I2C0_SCL	UART3 TXD signal	Y	+3,3V
A85	UART3_RXD	GP_C16/ GBE_MDIO/ PSE_UART3_RXD/ SIO_I2C0_SDA	UART3 RTS signal	Y	+3,3V
A98	UARTD_TXD (*) [2)]	GP_C21/ PSE_UART4_TXD/ SIO_UART2_TXD	UARTD TXD signal	Y	+3,3V
A99	UARTD_RXD (*) [2)]	GP_C20/ PSE_UART4_RXD/ SIO_UART2_RXD	UARTD RTS signal	Y	+3,3V

(*) UARTD is a UART Debug.

Note [1)]: UART0 and CAN1 cannot be mounted at the same time

Note [2)]: UARTD and CAN0 cannot be mounted at the same time

5.16 CAN (OPTION)

The CAN (Controller Area Network) peripheral is a serial communication bus designed for real-time applications. It enables the reliable transmission of data between different electronic devices, at high speed and with low power consumption.

The COMe Type 10 module does not include CANs, but they can be optional.

PIN	NAME	CPU PIN NAME	Description	TYPE	RAIL
A98	CAN0_TX [2)]	GP_E15/ PSE_I2S0_RXD/ PSE_CAN0_TX/ PSE_TGPIO17	CAN0 transmit signal	Y	+3,3V
A99	CAN0_RX [2)]	GP_E16/ PSE_I2S0_TXD/ PSE_CAN0_RX/ PSE_TGPIO16	CAN0 receive signal	Y	+3,3V
A101	CAN1_TX [1)]	GP_E20/ PSE_I2S0_SCLK/ PSE_CAN1_TX/ PSE_TGPIO14	CAN1 transmit signal	Y	+3,3V
A102	CAN1_RX [1)]	GP_E21/ PSE_I2S0_SFRM/ PSE_CAN0_RX/ PSE_TGPIO15	CAN1 receive signal	Y	+3,3V

Note [1)]: UART0 and CAN1 cannot be mounted at the same time

Note [2)]: UARTD and CAN0 cannot be mounted at the same time

CHAPTER 6

ON-LINE SUPPORT

We offer an on-line support to allow the customer to stay updated on the development of software release and on the enhancement of the documentation.

Following is shown the references for ENGICAM on-line support.

ENGICAM Product Experts are available to answer questions via email:

support@engicam.com

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In order to respect own internal policy regarding the environmental regulations and safety laws, Engicam confirms the compliant, of this product to the normatives ROHS and REACH and to the recognized hazards.

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