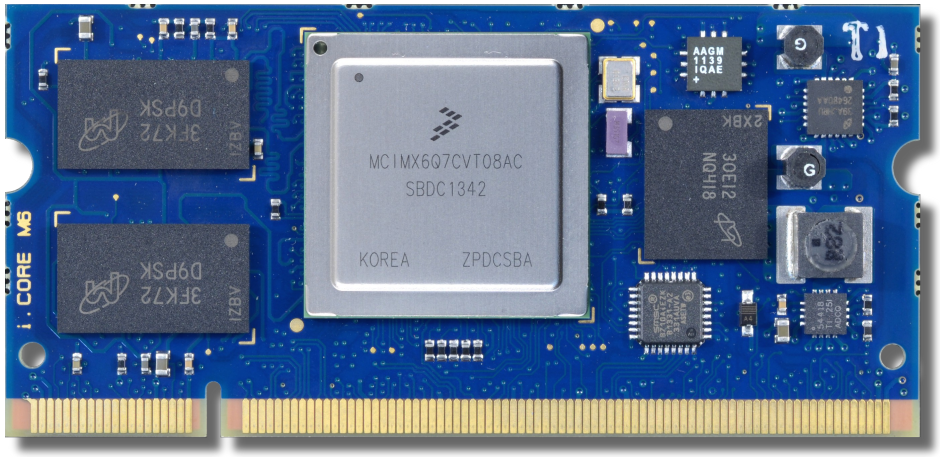
# i.Core M6S-DL-D-Q HW manual 2.0.9
# Getting started manual




***** REV 2.0.9 *****

| DATE | REVISION | CHANGE DESCRIPTION | |
|---|---|---|---|
| 27/12/12 | 1.0.0 | Release | |
| 31/12/13 | 1.1.5 | Added backup battery and CPU informations | |
| 19/06/14 | 1.1.6 | Updated pinout table and Ordering Information table | |
| 08/07/14 | 1.1.7 | Added Long Term Availability informations | |
| 19/09/14 | 1.1.8 | Updated the Ordering Code Table | |
| 22/01/15 | 2.0.0 | Updated Manual layout, added informations about USB OTG schemes | |
| 24/04/15 | 2.0.1 | Added informations about Ethernet protection, updated the ordering information | |
| 01/07/15 | 2.0.2 | Added Audio informations | |
| 07/08/15 | 2.0.3 | Added Ordering Code informations for modules with Yocto U-Boot | |
| 07/10/15 | 2.0.4 | Updated errata on ordering code table | |
| 23/11/15 | 2.0.5 | Updated ordering code table with RMA size info | |
| 05/01/16 | 2.0.6 | Added Reset pin informations | |
| 03/03/16 | 2.0.7 | General enhancement | |
| 13/05/16 | 2.0.8 | General enhancement | |
| 10/06/16 | 2.0.9 | Added information for PCIe design | |
| | | | |

# Summary

Chapter

1

# 1. Introduction

This Chapter gives background information on this document.

Section includes :

- ✔ **General Overview**
- ✔ **Acronyms and Abbreviations Used**
- ✔ **Document and Standard References**

## 1.1 Introduction

This document is created to guide users to design i.CoreM6 compliant carrier board. It will focus only on the interfaces in i.CoreM6 pinouts and related peripherals.

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

All examples of this document are based on i.CoreM6 carrier board that is available from ENGICAM. This document also provides a collection of useful documentation, application reports, and design recommendations.

## 1.2 Acronyms and Abbreviations used

| ABBREVIATION | EXPLANATION |
|---|---|
| ADC | Analogue to Digital Converter |
| CAN | Controller Area Network, a bus that is manly used in automotive and industrial environment |
| CPU | Central Processor Unit |
| DAC | Digital to Analogue Converter |
| EMI | Electromagnetic Interference, high frequency disturbances |
| eMMC | Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory |
| ESD | Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices |
| GND | Ground |
| GPIO | General Purpose Input/Output, pin that can be configured being an input or output |
| HDMI | High-Definition Multimedia Interface, combines audio and video signal |
| OTG | USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface |
| PCB | Printed Circuit Board |
| PD | Pull Down Resistor |
| PHY | Physical Layer of the OSI model |
| PMIC | Power Management IC, integrated circuit that manages amongst others the power sequence of a system |
| PU | Pull Up Resistor |
| PWM | Pulse-Width Modulation |
| RGB | Red Green Blue, colour channels in common display interfaces |
| SD | Secure Digital, flash memory card |
| SDIO | Secure Digital Input Output, an external bus for peripherals that uses the SD interface |
| SPI | Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals |
| USB | Universal Serial Bus, serial interface for internal and external peripherals |

## 1.3 Document and Standard References

### 1.3.1 External Industry Standard Documents

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- USB Specifications (www.usb.org).

### 1.3.2 NXP Documents

- IMX6DQRM
- IMX6SDLSRM
- IMX6DQAEC
- IMX6DQIEC
- IMX6DQCEC
- IMX6SDLAEC
- IMX6SDLIEC
- IMX6SDLCEC

http://www.NXP.com/webapp/sps/site/prod_summary.jsp?code=i.MX6Q&fpsp=1&tab=Documentation_Tab

## 1.4 Disclaimer

Information in this document is provided solely to enable system and software implementers to use Engicam products. Engicam does not guarantee that the information in this manual is up-to-date, correct, complete or of good quality. Nor does Engicam assume guarantee for further usage of the information.

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Chapter

2

# 2. Mechanical data

This Chapter gives information about PCB and module's dimensions.

Section includes :

- ✔ **Assembly Top**
- ✔ **Assembly Bottom**
- ✔ **Mechanical dimensions**

## 2.1 Mechanical data

The iMx6 module has a standard SO DIMM footprint compliant with TYCO ELECTRONICS code 1473005-1 or compatible connector. The PCB dimensions is L 67.60 x W 32.1 x H 1 mm. The distances available on PCB under the module are from 1 to 1,5 mm

## 2.2 Assembly Top View

The iMx6 Module has a Standard SODIMM footprint where odd pins are on top (component) side and even pins are on bottom side. In the Figure below is shown assembly and pin1 and pin 2 positions.

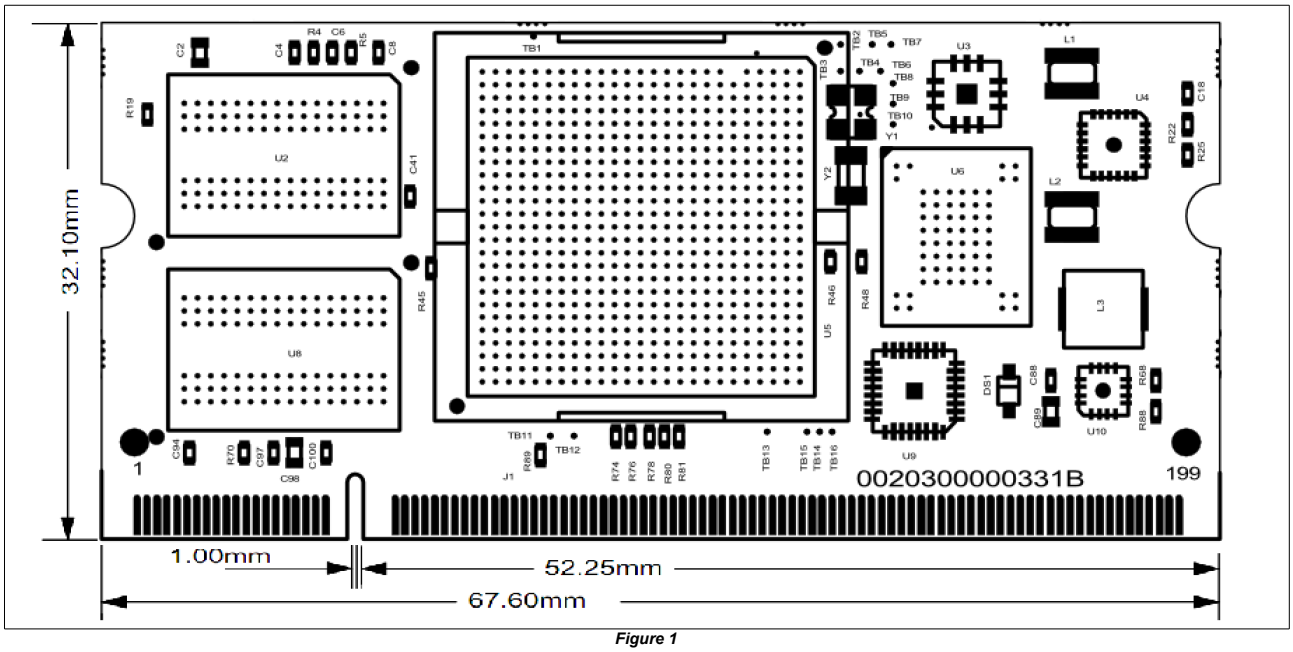


*Figure 1*

## 2.3 Assembly Bottom View

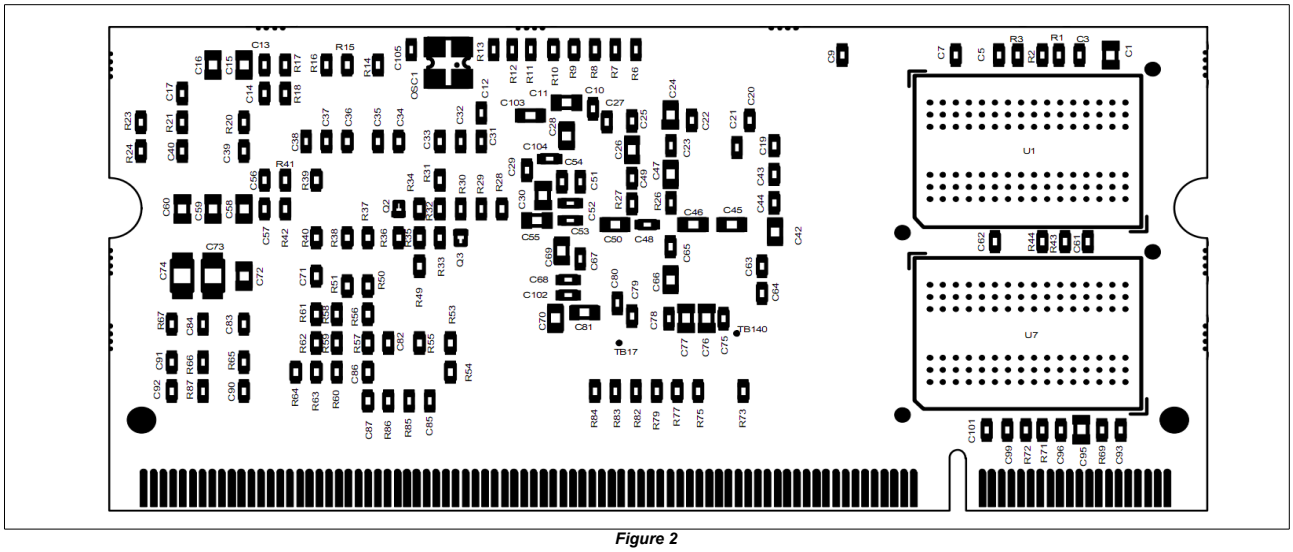

*Figure 2*

Chapter

3

# 3. Ordering Information and Features

This Chapter gives the ordering information and technical specifications of the modules.

Section includes :

- ✔ **i.CoreM6 Ordering code**
- ✔ **CPU & memory specifications**
- ✔ **Operating temperature range**
- ✔ **i.MX6 supported features**

## 3.1 Ordering Information (Yocto U-Boot)

Following is provided the ordering informations and the description for the Basic technical specifications modules:

| Marking Code | Ordering Code | MPQ | Description | CPU & Memory specifications | Operating temperature range °C (excepted CPU) | Module available at least until [1] |
|---|---|---|---|---|---|---|
| i.Core M6S | 00258000011010 | 1 | Module Sodimm i.CoreM6 Solo, 256MB DDR3, 512MB NAND, Industrial (Yocto U-Boot) | i.MX6 Solo Industrial Temperature **MCIMX6S7CVM08AC** 800MHz Industrial VPU/GPU, 512MB NAND, **-40 to +105C** [2] 32 bit Memory, temperature range industrial | -40 to +85 | 4thQ - 2027 |
| i.Core M6S | 00257000011010 | 58 | | | -40 to +85 | 4thQ - 2027 |
| i.Core M6S | 00257000011030 | - | Module Sodimm i.CoreM6 Solo, 256MB DDR3, 512MB NAND, Industrial, no touch (Yocto U-Boot) | | -40 to +85 | 4thQ - 2027 |
| i.Core M6S | 00258000011020 | 1 | Module Sodimm i.CoreM6 Solo, 256MB DDR3, 512MB NAND, Consumer, no touch (Yocto U-Boot) | i.MX6 Solo Extended Commercial Temperature **MCIMX6S5EVM10AC** 1 GHz Extended Commercial Temp VPU/GPU, 512MB NAND, **-20 to +105C** [2] 32 bit Memory, temperature range commercial | 0 to +70 | 4thQ - 2027 |
| i.Core M6S | 00257000011020 | 58 | | | 0 to +70 | 4thQ - 2027 |
| i.Core M6DL | 00258000011050 | 1 | Module Sodimm i.CoreM6 DualLite, 1GB RAM, 512MB NAND, Consumer, no touch (Yocto U-Boot) | i.MX6 DualLite Extended Commercial Temperature **MCIMX6U5EVM10AC** 1 GHz Ext Com Temp VPU/GPU, 512MB NAND, **-20 to +105C** [2] 64 bit Memory, temperature range commercial | 0 to +70 | 4thQ - 2027 |
| i.Core M6DL | 00257000011050 | 58 | | | 0 to +70 | 4thQ - 2027 |
| i.Core M6DL | 00257000011070 | 58 | Module Sodimm i.CoreM6 DualLite, 1GB DDR3, 512MB NAND, Industrial, no touch (Yocto U-Boot) | i.MX6 DualLite Industrial Temperature **MCIMX6U7CVM08AC** 800 MHz Ind Temp VPU/GPU, 512MB NAND, **-40 to +105C** [2] 64 bit Memory, temperature range industrial | -40 to +85 | 4thQ - 2027 |
| i.Core M6DL | 00258000011060 | 1 | Module Sodimm i.CoreM6 DualLite, 512MB DDR3, 512MB NAND, Consumer, no touch (Yocto U-Boot) | i.MX6 DualLite Extended Commercial Temperature **MCIMX6U5EVM10AC** 1 GHz Ext Con Temp VPU/GPU, 512MB NAND, **-20 to +105C** [2] 64 bit Memory, temperature range commercial | 0 to +70 | 4thQ - 2027 |
| i.Core M6DL | 00257000011060 | 58 | | | 0 to +70 | 4thQ - 2027 |
| i.Core M6D | 00258000011040 | 1 | Module Sodimm i.CoreM6 Dual, 512MB DDR3, 512MB NAND, Industrial (Yocto U-Boot) | i.MX6 Dual Industrial Temperature **MCIMX6D7CVT08AC** 800MHz Industrial VPU/GPU, 512MB NAND, **-40 to +105C** [2] 64 bit Memory temperature range industrial | -40 to +85 | 4thQ - 2027 |
| i.Core M6D | 00257000011040 | 58 | | | -40 to +85 | 4thQ - 2027 |
| i.Core M6Q | 00258000011080 | 1 | Module Sodimm i.CoreM6 Quad,1GB DDR3, 512MB NAND, Industrial (Yocto U-Boot) | i.MX6 Quad Industrial Temperature **MCIMX6Q7CVT08AC** 800MHz Industrial VPU/GPU, 512MB NAND, **-40 to +105C** [2] 64 bit Memory temperature range industrial | -40 to +85 | 4thQ - 2027 |
| i.Core M6Q | 00257000011080 | 58 | | | -40 to +85 | 4thQ - 2027 |

***Table 1***

[1] ***Long Term Availability based on NXP longevity program***
[2] ***Note: internal junction temperature***
***WARNING: the actual temperature depend on the application, the enclosure and/or the environmental condition. Upon customer to consider specific cooling solutions for its own final system.***

## 3.2 Ordering Information (LTIB U-Boot) *Following code are **NOT RECOMMENDED FOR NEW DESIGN***

| Marking Code | Ordering Code | MPQ | Description | CPU & Memory specifications | Operating temperature range °C (excepted CPU) | Module available at least until [1] |
|---|---|---|---|---|---|---|
| i.Core M6S | 00258000010650 | 1 | Module Sodimm i.CoreM6 Solo, 256MB DDR3, 512MB NAND, Industrial | i.MX6 Solo Industrial Temperature **MCIMX6S7CVM08AC** 800MHz Industrial VPU/GPU, 512MB NAND, **-40 to +105C** [2] 32 bit Memory, temperature range industrial | -40 to +85 | 4th Q - 2027 |
| i.Core M6S | 00257000010650 | 58 | | | -40 to +85 | 4th Q - 2027 |
| i.Core M6S | 00257000010170 | - | Module Sodimm i.CoreM6 Solo, 256MB DDR3, 512MB NAND, Industrial, no touch | | -40 to +85 | 4th Q - 2027 |
| i.Core M6S | 00258000010050 | 1 | Module Sodimm i.CoreM6 Solo no touch, 256MB DDR3, 512MB NAND, Consumer, no touch | i.MX6 Solo Extended Commercial Temperature **MCIMX6S5EVM10AC** 1 GHz Extended Commercial Temp VPU/GPU 512MB NAND, **-20 to +105C** [2] 32 bit Memory, temperature range commercial | 0 to +70 | 4th Q - 2027 |
| i.Core M6S | 00257000010050 | 58 | | | 0 to +70 | 4th Q - 2027 |
| i.Core M6DL | 00258000010260 | 1 | Module Sodimm i.CoreM6 DualLite, 1GB RAM, 512MB NAND, Consumer, no touch | i.MX6 DualLite Extended Commercial Temperature **MCIMX6U5EVM10AC** 1 GHz Ext Com Temp VPU/GPU, 512MB NAND, **-20 to +105C** [2] 64 bit Memory, temperature range commercial | 0 to +70 | 4th Q - 2027 |
| i.Core M6DL | 00257000010260 | 58 | | | 0 to +70 | 4th Q - 2027 |
| i.Core M6DL | 00257000010480 | 58 | Module Sodimm i.CoreM6 DualLite, 1GB DDR3, 512MB NAND, Industrial, no touch | i.MX6 DualLite Extended Commercial Temperature **MCIMX6U7CVM08AC** 800MHz Ext Ind Temp VPU/GPU, 512MB NAND, **-20 to +105C** [2] 64 bit Memory, temperature range Ind | -40 to +85 | 4th Q - 2027 |
| i.Core M6DL | 00258000010040 | 1 | Module Sodimm i.CoreM6 DualLite, 512MB DDR3, 512MB NAND, Consumer, no touch | i.MX6 DualLite Extended Commercial Temperature **MCIMX6U5EVM10AC** 1 GHz Ext Con Temp VPU/GPU, 512MB NAND, **-20 to +105C** [2] 64 bit Memory, temperature range commercial | 0 to +70 | 4th Q - 2027 |
| i.Core M6DL | 00257000010040 | 58 | | | 0 to +70 | 4th Q - 2027 |
| i.Core M6D | 00258000010360 | 1 | Module Sodimm i.CoreM6 Dual, 512MB DDR3, 512MB NAND, Industrial | i.MX6 Dual Industrial Temperature **MCIMX6D7CVT08AC** 800MHz Industrial VPU/GPU, 512MB NAND, **-40 to +105C** [2] 64 bit Memory temperature range industrial | -40 to +85 | 4th Q - 2027 |
| i.Core M6D | 00257000010360 | 58 | | | -40 to +85 | 4th Q - 2027 |
| i.Core M6Q | 00258000010090 | 1 | Module Sodimm i.CoreM6 Quad,1GB DDR3, 512MB NAND, Industrial | i.MX6 Quad Industrial Temperature **MCIMX6Q7CVT08AC** 800MHz Industrial VPU/GPU, 512MB NAND, **-40 to +105C** [2] 64 bit Memory temperature range industrial | -40 to +85 | 4th Q - 2027 |
| i.Core M6Q | 00257000010090 | 58 | | | -40 to +85 | 4th Q - 2027 |

***Table 2***

[1] **Long Term Availability based on NXP longevity program**
[2] ***Note: internal junction temperature***

***WARNING: the actual temperature depend on the application, the enclosure and/or the environmental condition. Upon customer to consider specific cooling solutions for its own final system.***

## 3.3 Comparison of Features and Functionalities

In the following table is summarized the key feature differences of i.MX 6Quad, i.MX 6Dual and i.MX 6Solo.

| Features | i.MX 6Quad | i.MX 6Dual | i.MX 6Solo |
|---|---|---|---|
| **Core** | Quad Cortex-A9, 800MHz | Dual Cortex-A9, 800MHz | Single Cortex-A9, 800MHz |
| **RAM** | 256 KB | 256 KB | 128 KB |
| **L2 cache** | 1 MB unified I/D L2 cache, shared by Quad core | 1 MB unified I/D L2 cache, shared by Dual core | 512 KB unified I/D L2 cache |
| **Image Processing Units** | Two autonomous and independent IPUs | Two autonomous and independent IPUs | One IPU |
| **Graphics acceleration** | Three independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with four shaders (up to 200 MT/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator | Three independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with four shaders (up to 200 MT/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator | Two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with one shader and a 2D graphics accelerator |
| **Displays** | Supports up to four displays at a time. Supported displays: parallel display, HDMI1.4, and 2 LVDS display | Supports up to four displays at a time. Supported displays: parallel display, HDMI1.4, and 2 LVDS display | Supports up to four displays at a time. Supported displays: parallel display, HDMI1.4, and 2 LVDS display |
| **Video input** | 1x CMOS camera INPUT 8bit | 1x CMOS camera INPUT 8bit | 1x CMOS camera INPUT 8bit |
| **SATA** | SATAII, 3.0 Gbps | SATAII, 3.0 Gbps | N/A |

***Table 3***

The modules as well as for the processors mounted by the three modules differ in the size of DDR3, for their access speed 64 or 32 bit and for the use of some peripherals as shown in the following table

| Features | i.MX 6Quad Module | i.MX 6Dual Module | i.MX 6Solo Module |
|---|---|---|---|
| **DDR Speed** | 64 bit | 64 bit | 32 bit |
| **DDR Size** | 1 GB | 512 | 256 |
| **SATA Interface** | yes | yes | Not present |
| **eCSPI** | eCSPI1 / eCSPI3 / eCSPI5 | eCSPI1 / eCSPI3 / eCSPI5 | eCSPI1 / eCSPI3 |

***Table 4***

**Note:** For further details and applications please refer to Hardware Migration for iMx6 document

Chapter

4

# 4. Pinout

This Chapter gives the pinout informations.

Section includes :

- ✔ **Pinout overview**
- ✔ **IMX Pad spacifications**

## 4.1 Module Pinout

The module's interface is achieved by a SO DIMM 200 position connector TYCO ELECTRONICS code 1473005-1 or compatible

| Pin | Name | Pin Name on I.MX6 | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|---|
| 1 | +1V8 [2] | - | Output Power PIN | - | - |
| 2 | +1V8 [2] | - | Output Power PIN | - | - |
| 3 | GND | - | Power PIN | N | - |
| 4 | GND | - | Power PIN | N | - |
| 5 | GND | - | Power PIN | N | - |
| 6 | CSI_D[12] | CSI0_DAT12 | CMOS Sensor Interface Data 12 | Y | +3,3V |
| 7 | CSI_D[13] | CSI0_DAT13 | CMOS Sensor Interface Data 13 | Y | +3,3V |
| 8 | CSI_D[14] | CSI0_DAT14 | CMOS Sensor Interface Data 14 | Y | +3,3V |
| 9 | CSI_D[15] | CSI0_DAT15 | CMOS Sensor Interface Data 15 | Y | +3,3V |
| 10 | CSI_D[16] | CSI0_DAT16 | CMOS Sensor Interface Data 16 | Y | +3,3V |
| 11 | CSI_D[17] | CSI0_DAT17 | CMOS Sensor Interface Data 17 | Y | +3,3V |
| 12 | CSI_D[18] | CSI0_DAT18 | CMOS Sensor Interface Data 18 | Y | +3,3V |
| 13 | CSI_D[19] | CSI0_DAT19 | CMOS Sensor Interface Data 19 | Y | +3,3V |
| 14 | CSI_VSYNC | CSI0_VSYNC | CMOS Sensor Interface Vertical Sync | Y | +3,3V |
| 15 | CSI_HSYNC | CSI0_MCLK | CMOS Sensor Interface Horizontal Sync | Y | +3,3V |
| 16 | CSI_CLK | CSI0_PIXCLK | CMOS Sensor Interface Pixel Clock | Y | +3,3V |
| 17 | NC | - | - | N | - |
| 18 | +Vcoin [3] | VDD_SNVS_IN | Backup battery or RTC | - | - |
| 19 | NC | - | - | - | - |
| 20 | NC | - | - | - | - |
| 21 | NC | - | - | - | - |
| 22 | GND | - | Power PIN | N | - |
| 23 | I2C3_SCL | GPIO_5 | I2C SCL Signal | Y | +3,3V |
| 24 | I2C3_SDA | EIM_D18 | I2C SDA Signal | Y | +3,3V |
| 25 | TOUCH_XP | - | Touch Screen Xp | - | +3,3V |
| 26 | TOUCH_XN | - | Touch Screen Xn | - | +3,3V |
| 27 | TOUCH_YP | - | Touch Screen Yp | - | +3,3V |
| 28 | TOUCH_YN | - | Touch Screen Yn | - | +3,3V |
| 29 | NC | - | - | - | - |
| 30 | NC | - | - | - | - |
| 31 | GND | - | Power PIN | N | - |
| 32 | NC | - | - | - | - |
| 33 | AD_AUX | - | - | - | +3,3V |
| 34 | GPIO_0 | GPIO_0 | Generic GPIO | Y | +3,3V |
| 35 | GPIO_2_SD2_WP | GPIO_2 | Generic GPIO | Y | +3,3V |
| 36 | GPIO_3 | GPIO_3 | Generic GPIO | Y | +3,3V |

| Pin | Name | Pin Name on I.MX6 | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|---|
| 37 | GPIO_4_SD2_CD | GPIO_4 | Generic GPIO | Y | +3,3V |
| 38 | GPIO_6 | GPIO_6 | Generic GPIO | Y | +3,3V |
| 39 | GND | - | Power PIN | - | - |
| 40 | GPIO_7 | GPIO_7 | Generic GPIO | Y | +3,3V |
| 41 | LVDS1_TX2_N | LVDS1_TX2_N | LVDS Interface's Signals | N | +2,5V |
| 42 | LVDS0_TX3_P | LVDS0_TX3_P | LVDS Interface's Signals | N | +2,5V |
| 43 | LVDS1_TX2_P | LVDS1_TX2_P | LVDS Interface's Signals | N | +2,5V |
| 44 | LVDS0_TX3_N | LVDS0_TX3_N | LVDS Interface's Signals | N | +2,5V |
| 45 | NC | - | - | - | - |
| 46 | LVDS0_CLK_P | LVDS0_CLK_P | LVDS Interface's Signals | N | +2,5V |
| 47 | LVDS1_TX3_N | LVDS1_TX3_N | LVDS Interface's Signals | N | +2,5V |
| 48 | LVDS0_CLK_N | LVDS0_CLK_N | LVDS Interface's Signals | N | +2,5V |
| 49 | LVDS1_TX3_P | LVDS1_TX3_P | LVDS Interface's Signals | N | +2,5V |
| 50 | LVDS0_TX1_P | LVDS0_TX1_P | LVDS Interface's Signals | N | +2,5V |
| 51 | LVDS1_TX1_N | LVDS1_TX1_N | LVDS Interface's Signals | N | +2,5V |
| 52 | LVDS0_TX1_N | LVDS0_TX1_N | LVDS Interface's Signals | N | +2,5V |
| 53 | LVDS1_TX1_P | LVDS1_TX1_P | LVDS Interface's Signals | N | +2,5V |
| 54 | LVDS1_TX0_N | LVDS1_TX0_N | LVDS Interface's Signals | N | +2,5V |
| 55 | LVDS1_CLK_N | LVDS1_CLK_N | LVDS Interface's Signals | N | +2,5V |
| 56 | LVDS1_TX0_P | LVDS1_TX0_P | LVDS Interface's Signals | N | +2,5V |
| 57 | LVDS1_CLK_P | LVDS1_CLK_P | LVDS Interface's Signals | N | +2,5V |
| 58 | LVDS0_TX2_P | LVDS0_TX2_P | LVDS Interface's Signals | N | +2,5V |
| 59 | LVDS0_TX0_P | LVDS0_TX0_P | LVDS Interface's Signals | N | +2,5V |
| 60 | LVDS0_TX2_N | LVDS0_TX2_N | LVDS Interface's Signals | N | +2,5V |
| 61 | LVDS0_TX0_N | LVDS0_TX0_N | LVDS Interface's Signals | N | +2,5V |
| 62 | GPIO_SP1 | CSI0_DAT5 | CMOS Sensor Interface Data 4 | Y | +3,3V |
| 63 | EIM_A16 [7] | EIM_A16 | External Interface Module | Y | +3,3V |
| 64 | GND | - | Power PIN | N | - |
| 65 | EIM_A17 [7] | EIM_A17 | External Interface Module | Y | +3,3V |
| 66 | GPIO_SP2 | CSI0_DAT6 | GPIO Spare | Y | +3,3V |
| 67 | PCIe_RXM | PCIe_RXM | PCIe Interface | N | - |
| 68 | GPIO_SP3 | CSI0_DAT7 | GPIO Spare | Y | +3,3V |
| 69 | PCIe_RXP | PCIe_RXP | PCIe Interface | N | - |
| 70 | HDMI_HPD | HDMI_HPD | HDMI Interface | N | - |
| 71 | GND | - | Power PIN | N | - |
| 72 | PCIe_TXM | PCIe_TXM | PCIe Interface | N | - |
| 73 | HDMI_CECIN | EIM_A25 | HDMI Interface | Y | +3,3V |
| 74 | PCIe_TXP | PCIe_TXP | PCIe Interface | N | - |
| 75 | HDMI_CLKM | HDMI_CLKM | HDMI Interface | N | - |
| 76 | PCIe_REFCLKM | CLK1_N | PCIe Interface | N | - |

| Pin | Name | Pin Name on I.MX6 | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|---|
| 77 | HDMI_CLKP | HDMI_CLKP | HDMI Interface | N | - |
| 78 | PCIe_REFCLKP | CLK1_P | PCIe Interface | N | - |
| 79 | EIM_D29 [2] | EIM_D29 | External Interface Module | - | - |
| 80 | EIM_DA7 [1] | EIM_DA7 | External Interface Module | Y | +3,3V |
| 81 | HDMI_D0M | HDMI_D0M | HDMI Interface | N | - |
| 82 | EIM_A19 [1] | EIM_A19 | External Interface Module | Y | +3,3V |
| 83 | HDMI_D0P | HDMI_D0P | HDMI Interface | N | - |
| 84 | EIM_A20 [1] | EIM_A20 | External Interface Module | Y | +3,3V |
| 85 | HDMI_D1M | HDMI_D1M | HDMI Interface | N | - |
| 86 | EIM_A21 [1] | EIM_A21 | External Interface Module | Y | +3,3V |
| 87 | HDMI_D1P | HDMI_D1P | HDMI Interface | N | - |
| 88 | EIM_A22 [1] | EIM_A22 | External Interface Module | Y | +3,3V |
| 89 | GND | - | Power PIN | N | - |
| 90 | EIM_A23 [1] | EIM_A23 | External Interface Module | Y | +3,3V |
| 91 | HDMI_D2M | HDMI_D2M | HDMI Interface | N | - |
| 92 | EIM_A24 [1] | EIM_A24 | External Interface Module | Y | +3,3V |
| 93 | HDMI_D2P | HDMI_D2P | HDMI Interface | N | - |
| 94 | EIM_D16 | EIM_D16 | External Interface Module | Y | +3,3V |
| 95 | NC | - | - | - | - |
| 96 | NC | - | - | - | - |
| 97 | DI0_PIN4 [2] | DI0_PIN4 | Image Processing Unit signal | Y | +3,3V |
| 98 | NC | - | - | - | - |
| 99 | NC | - | - | - | - |
| 100 | NC | - | - | - | - |
| 101 | SATA_RXM | SATA_RXM | SATA Interface | N | - |
| 102 | SATA_TXP | SATA_TXP | SATA Interface | N | - |
| 103 | SATA_RXP | SATA_RXP | SATA Interface | N | - |
| 104 | SATA_TXM | SATA_TXM | SATA Interface | N | - |
| 105 | UART3_CTS | EIM_D23 | UART3 CTS signal | Y | +3,3V |
| 106 | UART3_RTS [1] | EIM_EB3 | UART3 RTS signal | Y | +3,3V |
| 107 | GND | - | Power PIN | N | - |
| 108 | UART3_TXD | EIM_D24 | UART3 TXD signal | Y | +3,3V |
| 109 | UART3_RXD | EIM_D25 | UART3 RXD signal | Y | +3,3V |
| 110 | I2C2_SDA | KEY_ROW3 | I2C SDA Signal | Y | +3,3V |
| 111 | I2C2_SCL | KEY_COL3 | I2C SCL Signal | Y | +3,3V |
| 112 | UART2_TXD | EIM_D26 | UART2 TXD signal | Y | +3,3V |
| 113 | UART2_RXD | EIM_D27 | UART2 RXD signal | Y | +3,3V |
| 114 | I2S_DIN | DISP0_DAT23 | I2S Data In | Y | +3,3V |
| 115 | I2S_LRCLK | DISP0_DAT22 | I2S RCLK | Y | +3,3V |
| 116 | UART4_TX | KEY_COL0 | UART4 TXD signal | Y | +3,3V |

| Pin | Name | Pin Name on I.MX6 | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|---|
| 117 | UART4_RX | KEY_ROW0 | UART4 RXD signal | Y | +3,3V |
| 118 | CAN1_TX | KEY_COL2 | CAN 1 transmit signal | Y | +3,3V |
| 119 | CAN1_RX | KEY_ROW2 | CAN 1 receive signal | Y | +3,3V |
| 120 | CAN2_TX | KEY_COL4 | CAN 2 transmit signal | Y | +3,3V |
| 121 | CAN2_RX | KEY_ROW4 | CAN 2 receive signal | Y | +3,3V |
| 122 | I2S_DOUT | DISP0_DAT21 | I2S Data Out | Y | +3,3V |
| 123 | GND | - | Power PIN | N | - |
| 124 | I2S_SCLK | DISP0_DAT20 | I2S SCLK | Y | +3,3V |
| 125 | DISP0_CLK | DI0_DISP_CLK | LCD interface | Y | +3,3V |
| 126 | NC | - | - | - | - |
| 127 | ETH_TXN | - | Fast Ethernet TXN signal | - | - |
| 128 | nRESET | POR_B | Reset signal | N | +3,3V |
| 129 | ETH_TXP | - | Fast Ethernet TXP signal | - | - |
| 130 | GPIO_SP0 | CSI0_DAT4 | GPIO Spare | Y | - |
| 131 | ETH_RXN | - | Fast Ethernet RXN signal | - | - |
| 132 | DISP0_CONTRAST [2] | SD4_DAT1 | LCD interface | Y | +3,3V |
| 133 | ETH_RXP | - | Fast Ethernet RXP signal | - | - |
| 134 | +3V3_OUT | - | Output Power PIN | N | - |
| 135 | +3V3_OUT | - | Output Power PIN | N | - |
| 136 | NC | - | - | - | - |
| 137 | ETH_LED_10_100_KATHOD | - | Led Indicator Cathode signal | - | - |
| 138 | NC | - | - | - | - |
| 139 | ETH_LED_ACT_ANOD | - | Led indicator Anode signal | - | - |
| 140 | +3V3_OUT | - | Output Power PIN | - | - |
| 141 | DISP0_D17 | DISP0_DAT17 | LCD interface | Y | +3,3V |
| 142 | DISP0_D16 | DISP0_DAT16 | LCD interface | Y | +3,3V |
| 143 | DISP0_D15 | DISP0_DAT15 | LCD interface | Y | +3,3V |
| 144 | DISP0_D14 | DISP0_DAT14 | LCD interface | Y | +3,3V |
| 145 | DISP0_D13 | DISP0_DAT13 | LCD interface | Y | +3,3V |
| 146 | DISP0_D12 | DISP0_DAT12 | LCD interface | Y | +3,3V |
| 147 | DISP0_D11 | DISP0_DAT11 | LCD interface | Y | +3,3V |
| 148 | DISP0_D10 | DISP0_DAT10 | LCD interface | Y | +3,3V |
| 149 | DISP0_D9 | DISP0_DAT9 | LCD interface | Y | +3,3V |
| 150 | DISP0_D8 | DISP0_DAT8 | LCD interface | Y | +3,3V |
| 151 | DISP0_D7 | DISP0_DAT7 | LCD interface | Y | +3,3V |
| 152 | DISP0_D6 | DISP0_DAT6 | LCD interface | Y | +3,3V |
| 153 | DISP0_D5 | DISP0_DAT5 | LCD interface | Y | +3,3V |
| 154 | DISP0_D4 | DISP0_DAT4 | LCD interface | Y | +3,3V |
| 155 | DISP0_D3 | DISP0_DAT3 | LCD interface | Y | +3,3V |
| 156 | GND | - | Power PIN | N | - |

| Pin | Name | Pin Name on I.MX6 | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|---|
| 157 | DISP0_D2 | DISP0_DAT2 | LCD interface | Y | +3,3V |
| 158 | DISP0_D1 | DISP0_DAT1 | LCD interface | Y | +3,3V |
| 159 | DISP0_D0 | DISP0_DAT0 | LCD interface | Y | +3,3V |
| 160 | DISP0_VSYNC | DI0_PIN3 | LCD interface | Y | +3,3V |
| 161 | DISP0_HSYNC | DI0_PIN2 | LCD interface | Y | +3,3V |
| 162 | DISP0_DRDY | DI0_PIN15 | LCD interface | Y | +3,3V |
| 163 | NC | - | - | - | - |
| 164 | NC | - | - | - | - |
| 165 | NC | - | - | - | - |
| 166 | SD2_D3 | SD2_DAT3 | eSDHC 2 DAT 3 signal | Y | +3,3V |
| 167 | SD2_CMD | SD2_CMD | eSDHC 2 CMD signal | Y | +3,3V |
| 168 | SD2_D0 | SD2_DAT0 | eSDHC 2 DAT 0 signal | Y | +3,3V |
| 169 | SD2_CLK | SD2_CLK | eSDHC 2 CLK signal | Y | +3,3V |
| 170 | SD2_D2 | SD2_DAT2 | eSDHC 2 DAT 2 signal | Y | +3,3V |
| 171 | SD2_D1 | SD2_DAT1 | eSDHC 2 DAT 1 signal | Y | +3,3V |
| 172 | NC | - | - | - | - |
| 173 | JTAG_TRSTB | JTAG_TRSTB | JTAG Interface | N | +3,3V |
| 174 | JTAG_TDO | JTAG_TDO | JTAG Interface | N | +3,3V |
| 175 | JTAG_TDI | JTAG_TDI | JTAG Interface | N | +3,3V |
| 176 | JTAG_TMS | JTAG_TMS | JTAG Interface | N | +3,3V |
| 177 | JTAG_TCK | JTAG_TCK | JTAG Interface | N | +3,3V |
| 178 | NC | - | - |  | - |
| 179 | JTAG_nSRST | POR_B | JTAG Interface with Pull-up on module | N | +3,3V |
| 180 | USB_H1_VBUS | USBH1_VBUS | USB HOST interface | N | - |
| 181 | BOOT_MODE | - | Boot from USB UART or on board Nand Flash | - | - |
| 182 | GND | - | Power PIN | N | - |
| 183 | GPIO_1_SD1_CD | GPIO_1 | eSDHC CD Signal | Y | +3,3V |
| 184 | GPIO_9_SD1_WP | GPIO_9 | eSDHC WP Signal | Y | +3,3V |
| 185 | SD1_D2 | SD1_DAT2 | eSDHC DAT 2 signal | Y | +3,3V |
| 186 | SD1_D3 | SD1_DATA3 | eSDHC DAT 3 signal | Y | +3,3V |
| 187 | SD1_D1 | SD1_DATA1 | eSDHC DAT 1 signal | Y | +3,3V |
| 188 | SD1_D0 | SD1_DATA0 | eSDHC DAT 0 signal | Y | +3,3V |
| 189 | SD1_CLK | SD1_CLK | eSDHC CLK signal | Y | +3,3V |
| 190 | SD1_CMD | SD1_CMD | eSDHC CMD signal | Y | +3,3V |
| 191 | USB_OTG_ID [4] | ENET_RX_ER | USB on the go interface | Y | +3,3V |
| 192 | USB_OTG_DP | USB_OTG_DP | USB on the go interface | N | - |
| 193 | USB_OTG_DN | USB_OTG_DN | USB on the go interface | N | - |
| 194 | USB_H1_DP | USB_HI_DP | USB HOST interface | N | - |
| 195 | USB_OTG_VBUS | USB_OTG_VBUS | USB on the go interface | N | - |
| 196 | USB_H1_DN | USB_H1_DN | USB HOST interface | N | - |

| Pin | Name | Pin Name on I.MX6 | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|---|
| 197 | +5Vin | - | Power PIN | N | - |
| 198 | +5Vin | - | Power PIN | N | - |
| 199 | +5Vin | - | Power PIN | N | - |
| 200 | +5Vin | - | Power PIN | N | - |

*Table 5*

[1] *Note: for the use of this pin please refer to boot option in "**Boot Mode Pin"** chapter*

[2] *Note: available from the module PCB i.CoreM6 REV C*

[3] *Connect to Coin-Cell or Super-Cap; left floating if not use*

[4] *Refer to PCN_1405-1_EN and to PCN_1405-2_EN*

**The yellow lines highlight the required minimum electrical connections in order to make the module working correctly.**

Chapter

5

# 5. Carrier Board Design

This Chapter gives the technical specifications for carrier board design.

Section includes :

- ✔ **Carrier Board recommendations**
- ✔ **Power signals and backup battery**
- ✔ **Serials**
- ✔ **CAN Bus**
- ✔ **Ethernet**
- ✔ **USB**
- ✔ **SDIO**
- ✔ **LCD and LVDS**
- ✔ **SATA**
- ✔ **PCIe**
- ✔ **Jtag interface**
- ✔ **Boot mode**
- ✔ **Touch screen controller**
- ✔ **Audio**
- ✔ **Reset pin management**

## 5.1 Carrier board recommended specifications

Following we'll describe the specifications required to carrier board to avoid problems of assembly process. The module is interfaced with the carrier board through a SO-DIMM with 200 positions connector type TYCO ELECTRONICS code 1473005-1 or compatible.
For proper assembly is strongly recommended to paying attention to:

### 5.1.1 Planarity in finish process

Due to the technical and mechanical specifications of the connector we suggest the maximum planarity of the footprint on PCB, so we suggest a type of finish obtained by horizontal process ( we suggest and use for our carrier boards a type Chemical Gold finish).

### 5.1.2 Planarity of PCB

Also the planarity of the entire Printed Circuit Board must be kept in check especially when the your carrier board grows in size. In this case we suggest you contact the manufacturer of PCB to understand how improve the planarity of ended board and optimize the process maintaining the electrical characteristics unchanged

*Note: for further detail please refer to your SO-DIMM connector's data-sheet*

### 5.1.3 Power Supply

It's strongly recommended that the power supply of the carrier board, which feeds the driver and control devices connected with the iMx processor, begins to work after the initialization of the processor itself

## 5.2 How to power the iMX6 module

Please read carefully the related sections before start your power stage design. This module needs to be supply up to +5Vin power. Please refer to the table below for the power supply range specification. The power dissipated by the module in the operating mode is about 250-350 mA, but **the system must provide at least a power of 2A at 5V to allow the start of the module.**

| | Min | Typ | Max |
|---|---|---|---|
| Voltage range | - | +5V | +5,5V |
| i.CoreM6S Current @ 5,0V | - | 250 mA | - |
| i.CoreM6DL Current @ 5,0V | - | 280 mA | - |
| i.CoreM6D Current @ 5,0V | - | 300 mA | - |
| i.CoreM6Q Current @ 5,0V | - | 350 mA | - |

*Table 6*

***Note:*** *the measure of table above are to be considered referred to the module with only the Linux OS running, the use of graphic accelerators or other multimedia applications could be cause of higher consumption than those indicated.*

In the following table are shown the module power supply pins numbering, please connect all power supply pins in order to avoid damage.

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 197 | +5Vin | Power PIN | N | - |
| 198 | +5Vin | Power PIN | N | - |
| 199 | +5Vin | Power PIN | N | - |
| 200 | +5Vin | Power PIN | N | - |
| 3 | GND | Power PIN | N | - |
| 4 | GND | Power PIN | N | - |
| 5 | GND | Power PIN | N | - |
| 22 | GND | Power PIN | N | - |
| 31 | GND | Power PIN | N | - |
| 39 | GND | Power PIN | N | - |
| 64 | GND | Power PIN | N | - |
| 71 | GND | Power PIN | N | - |
| 89 | GND | Power PIN | N | - |
| 107 | GND | Power PIN | N | - |
| 123 | GND | Power PIN | N | - |
| 156 | GND | Power PIN | N | - |
| 182 | GND | Power PIN | N | - |

*Table 7*

iMx6 module has 5 Output power PIN usable for power source. In the table below are shown the power supply pins numbering.

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 1 | +1V8 | Output Power PIN | N | - |
| 2 | +1V8 | Output Power PIN | N | - |
| 134 | +3V3_OUT | Output Power PIN | N | - |
| 135 | +3V3_OUT | Output Power PIN | N | - |
| 140 | +3V3_OUT | Output Power PIN | N | - |

*Table 8*

In the following table are shown the nominal maximum rating of power output:

| Power output | Max output current |
|---|---|
| +1V8 | 200 mA (Total) |
| +3V3_OUT | 1000 mA (Total) |

*Table 9*

***WARNING!***

*The currents above 600 mA provided by the +3V3_OUT of the module, help to lower the performance in temperature.*
*We recommend to add a regulator voltage for an external current greater than or equal to 600 mA, in those applications where the operating temperature range is important.*

***For further details on the power supply please refer to "i.CoreM6" data sheet and Reference Manual.***

### 5.2.1 How to connect a backup battery

The module allows the use of lithium rechargeable battery or supercapacitor as backup battery.
The connection with module is obtained by connecting directly the backup battery to the +Vcoin signal (pin 18 floating if not used).

The consumption of the pin is given by NXP for a maximum of 275uA

**Note:** *The module is already designed to manage the charge of backup battery.*

## 5.3 How to connect two 3-wire RS232 serial port

In this section is shown how to use the iMx6 UART1 and UART2 as 3-wire RS232 serial ports.
In the following table are shown the UART1 and UART2 pins numbering.

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 112 | UART2_TXD | UART2 TXD signal | Y | +3,3V |
| 113 | UART2_RXD | UART2 RXD signal | Y | +3,3V |
| 116 | UART4_TXD * | UART4 TXD signal | Y | +3,3V |
| 117 | UART4_RXD * | UART4 RXD signal | Y | +3,3V |

*Table 10*

The signal on the module's UART pins are 3.3V logic level, this can not be connected directly to a RS232 device like a PC Serial port, the use of a transceivers on the base board is mandatory in order to avoid module damage.

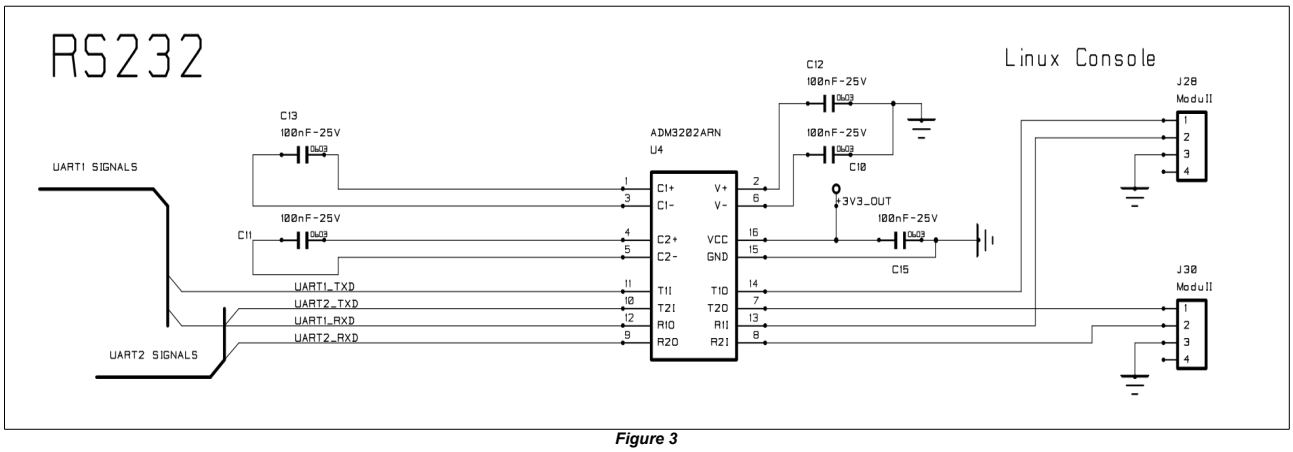


*Figure 3*

In the previous figure is shown how **UART4** ( label UART1 in the figure referred to the EVA BOARD) and UART2 are connected in the iMx6 evaluation board. In this example an ADM3202ARN IC from Analog Device is used like transceiver for both UART without any control signal. In case RTS and CTS are need, a transceiver must be used for this signals.

When Linux is installed on a module, UART4 is used like console. The default communications settings is shown in the table below.

| Linux console default settings | |
|---|---|
| Baud rate | 115200 |
| Data length | 8 bit |
| Parity | none |
| Stop | 1bit |

*Table 11*

* **Note**: *the UART4 is used as Linux Console*

## 5.4 How to connect a RS485 serial port

In this chapter is shown how an RS485 serial port can be connected to the module. In the figure below is shown how UART3 is used to connect to a RS485 transceiver on the starter kit. The figure shows UART3 connection but you can consider that also UART 4 & 5 can be used to connect a RS485 transceiver.

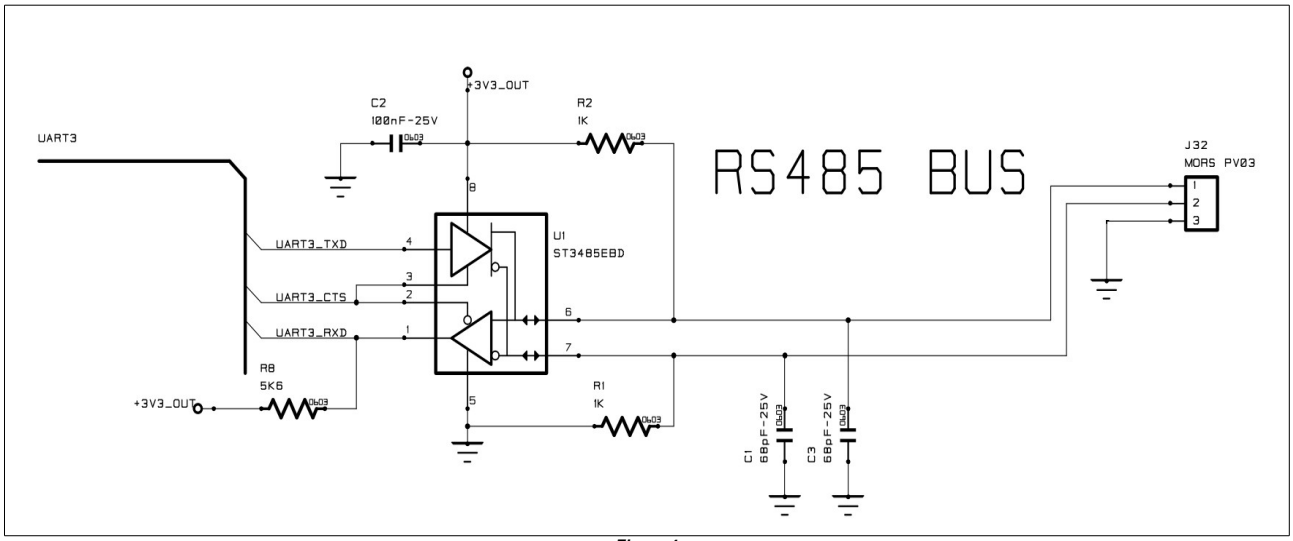


*Figure 4*

The pins involved in this RS485 communication example are listed in the following table.

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 105 | UART3_CTS | UART3 CTS signal | Y | +3,3V |
| 106 | UART3_RTS | UART3 RTS signal | Y | +3,3V |
| 108 | UART3_TXD | UART3 TXD signal | Y | +3,3V |
| 109 | UART3_RXD | UART3 RXD signal | Y | +3,3V |

*Table 12*

## 5.5 How to connect CAN BUS interfaces

In this chapter is described how CAN bus transceiver can be connected to a iMx6 module. In the figure below is shown how CAN bus1 and 2 are connected in the evaluation board. Both CAN buses have been implemented.

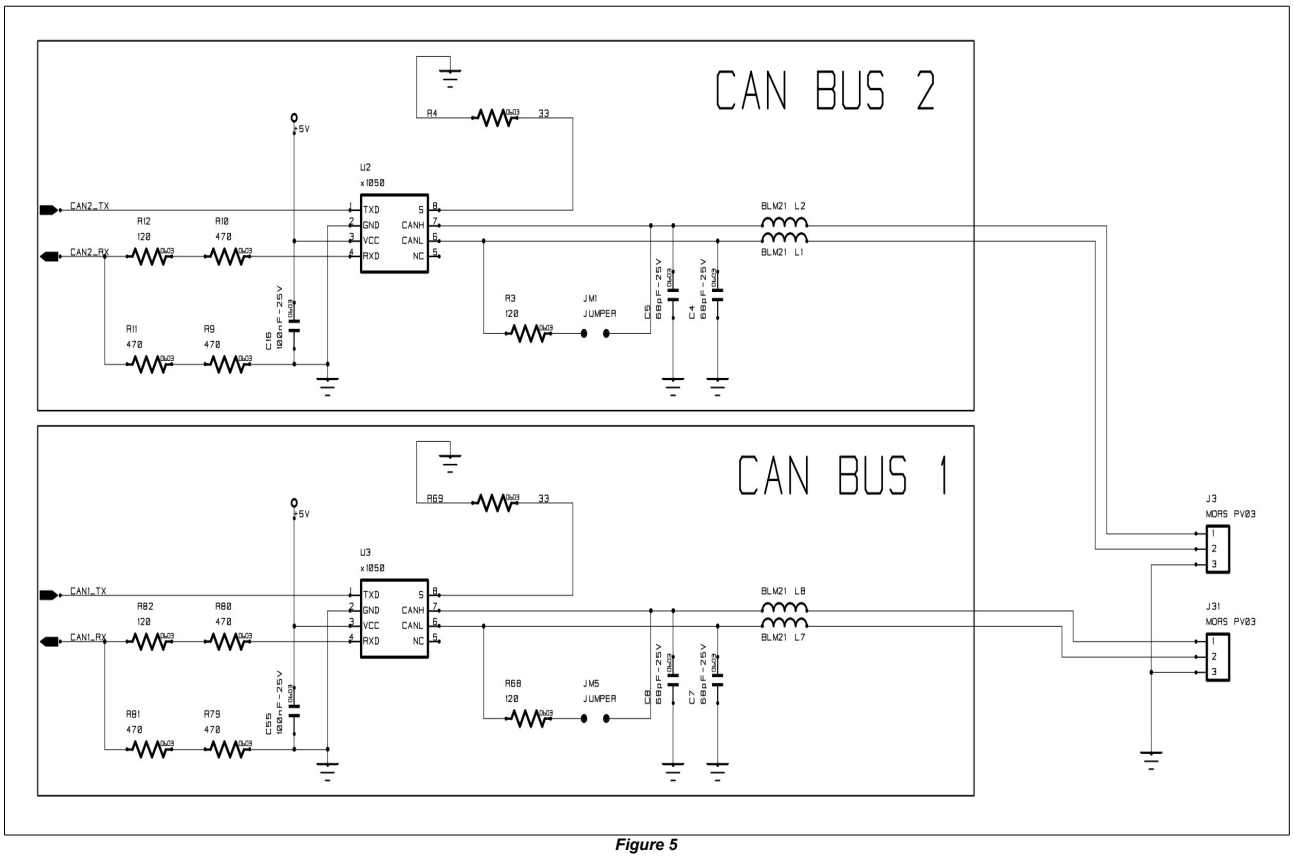


*Figure 5*

The following table describes the pins' numbering in the main connector involved in the CAN interface

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 118 | CAN1_TX | CAN 1 transmit signal | Y | +3,3V |
| 119 | CAN1_RX | CAN 1 receive signal | Y | +3,3V |
| 120 | CAN2_TX | CAN 2 transmit signal | Y | +3,3V |
| 121 | CAN2_RX | CAN 2 receive signal | Y | +3,3V |

*Table 13*

The Jumpers JM1, JM5 are used to close the load of the CAN Bus to 120 Ω

## 5.6 How to design the Ethernet interface

The NXP iMx6 Ethernet Media Access Controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE standard 802.3™ networks. The 10-Mbps and 100-Mbps RMII Ethernet physical interfaces is supported. In the figure is shown how to connect the Ethernet interface to module.

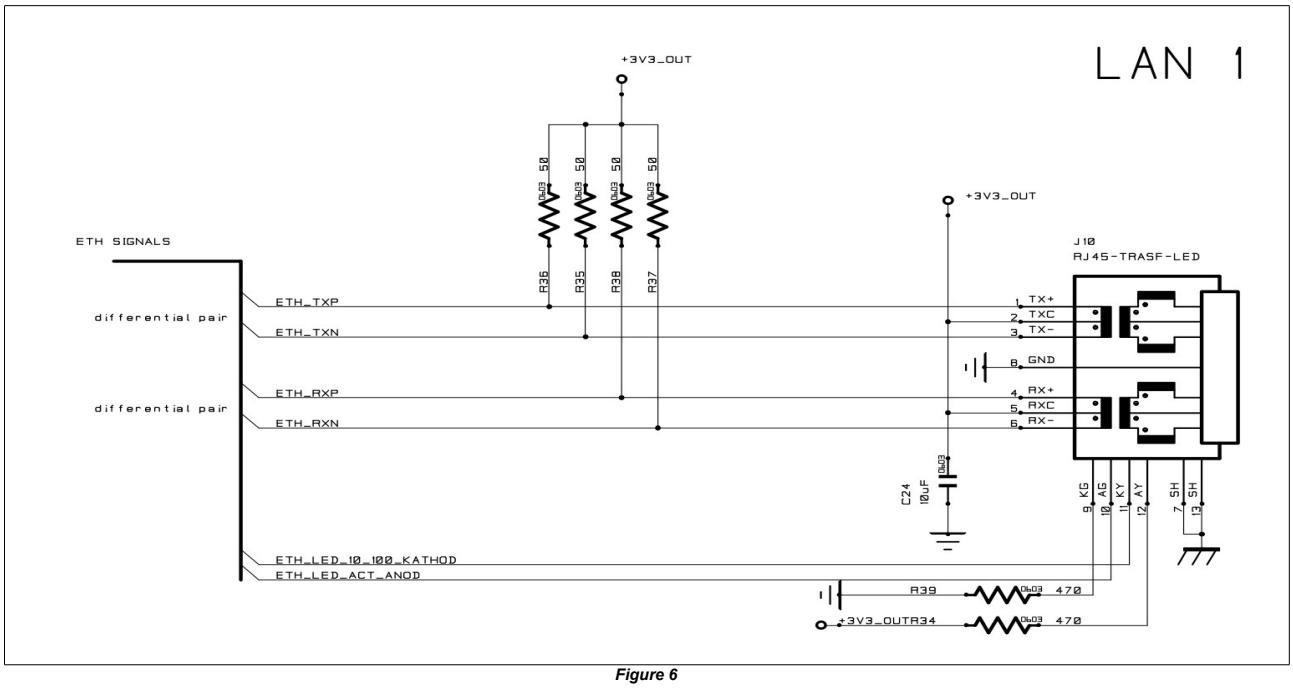


*Figure 6*

In the table below are listed all Ethernet signal of the module:

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 127 | ETH_TXN | Fast Ethernet TXN signal | - | +3,3V |
| 129 | ETH_TXP | Fast Ethernet TXP signal | - | +3,3V |
| 131 | ETH_RXN | Fast Ethernet RXN signal | - | +3,3V |
| 133 | ETH_RXP | Fast Ethernet RXP signal | - | +3,3V |
| 137 * | ETH_LED_10_100_KATHOD | Led Indicator Cathode signal | - | +3,3V |
| 139 * | ETH_LED_ACT_ANOD | Led indicator Anode signal | - | +3,3V |

*Table 14*

* ***Note:*** If not used, this pin must be left floating.

## 5.6.1 Component Placement considerations

Components placement can affect signal quality, emissions and can decrease EMI problems.

1. If the magnetics are a discrete component than the distance from the connector RJ45 should be kept to under 25mm of separation.
2. To decrease EMI problems the distance between magnetics and Phy should be at least 25mm or greater to isolate the PHY from magnetics.
3. The distance between Phy and RJ45 connector should always be within 200 mm.
4. The differential transmit pair should be keep at least 25mm from the edge of PCB up to the magnetics. If the magnetics are integrated into RJ45 the differential pair should be routed to the back of integrated magnetics RJ45 connector , away from the board of PCB.
5. The 49.9 ohm pull-up resistors on the differential lines should be placed within 10 mm of the Phy device
6. The signals RX & TX should be independently matched in length to within 6mm

See following figure

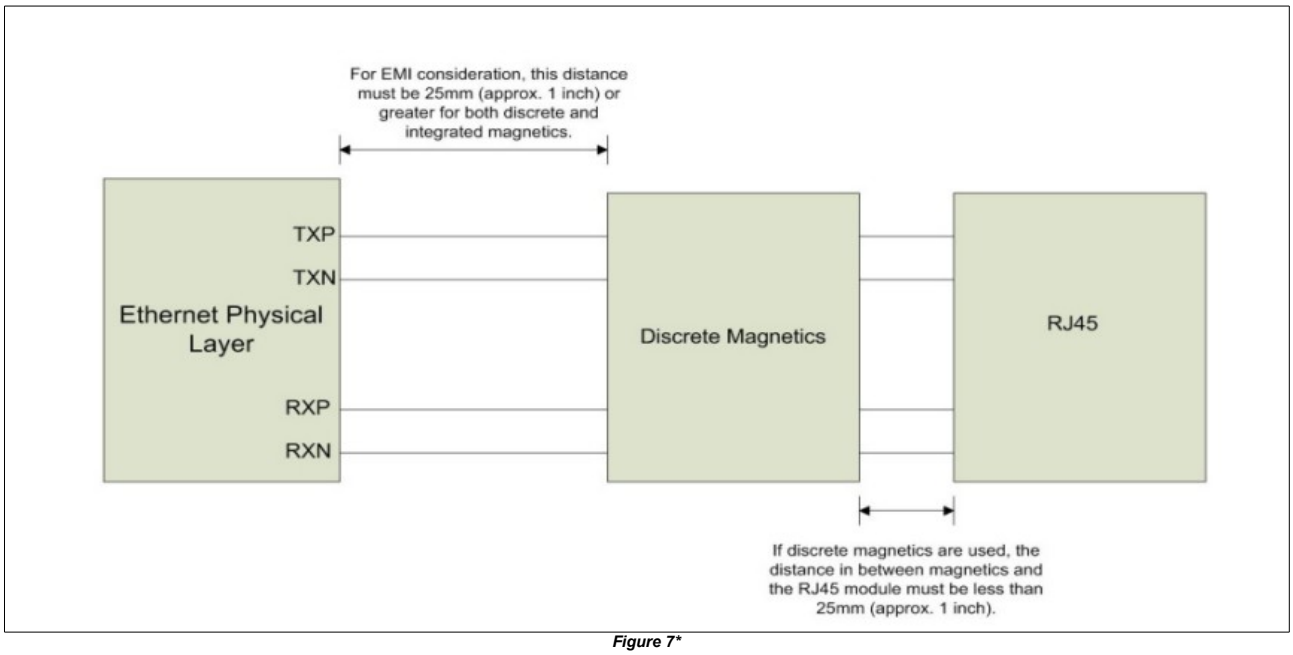


***Figure 7****

The PHY used in the module is the ***SMSC LAN8710***.
Please for more information refer to the ***SMSC Ethernet Physical Layer Layout Guidelines***.

For a list of magnetics selected to operate with the SMSC LAN8710, please refer to the Application note ***AN 8-13 Suggested Magnetics.***

*** this is the figure 2.3 from SMSC Ethernet Physical Layer Layout Guidelines**

### 5.6.2 Cable Transient Event and PHY Protection

Cable transient events are + and - DC surges that are induced across the transformer onto the PHY side of the TX+/- and RX+/- signals as shown in figure below. The PHY side of the transformer should not contain any DC component other than the typical 3.3V pull-up on the center tap of the transformer for analog signal biasing. Especially in POE applications, there are two main reasons why cable transient events occur, negative rail PSE switching, and hot unplug/plug-in events.

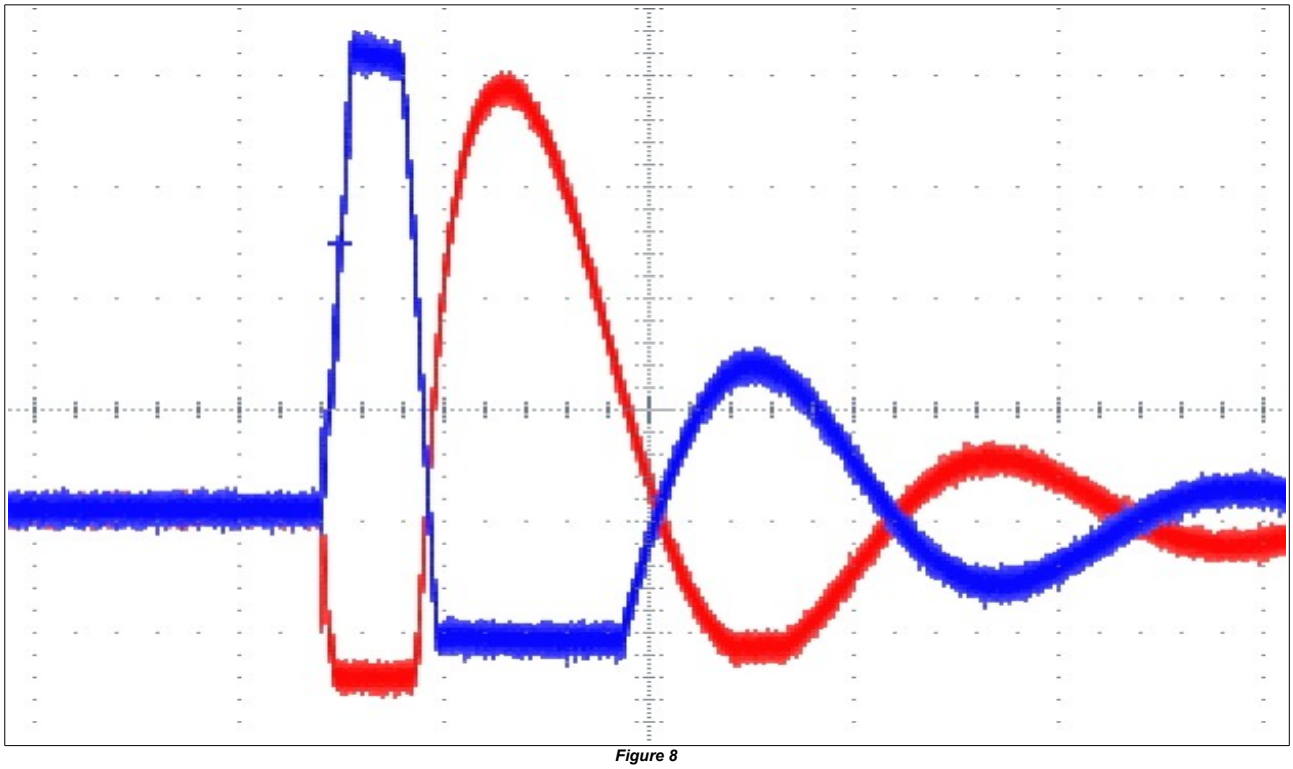

*Figure 8*

Transient observer on the PHY side of Eth Magnetics

Scale X = 1uS/div

Scale Y = 5V/div

**Note:** *for further details about Cable transient events please refers to file AN1718 of SMSC*

## 5.6.3 Phy Ethernet

When using an SMSC device, for each application an external transient protection is recommended , especially when the POE is used, as shown in figure below. The schematic shows an example of a TVS suppression solution. This solution couples the energy differentially into the two TVS diodes on each differential pair. For cases when the transient is across the TX+/- pair in the figure below, the voltage is clamped at a value equivalent to the forward bias voltage across D1, plus the zener voltage of D2. This transient voltage must be clamped at a voltage no **greater than 5V**. D3 and D4 act the same way when the transient is across the RX+/- differential pair. The total capacitance seen by each differential pair must not exceed 50pF (25pF single ended).

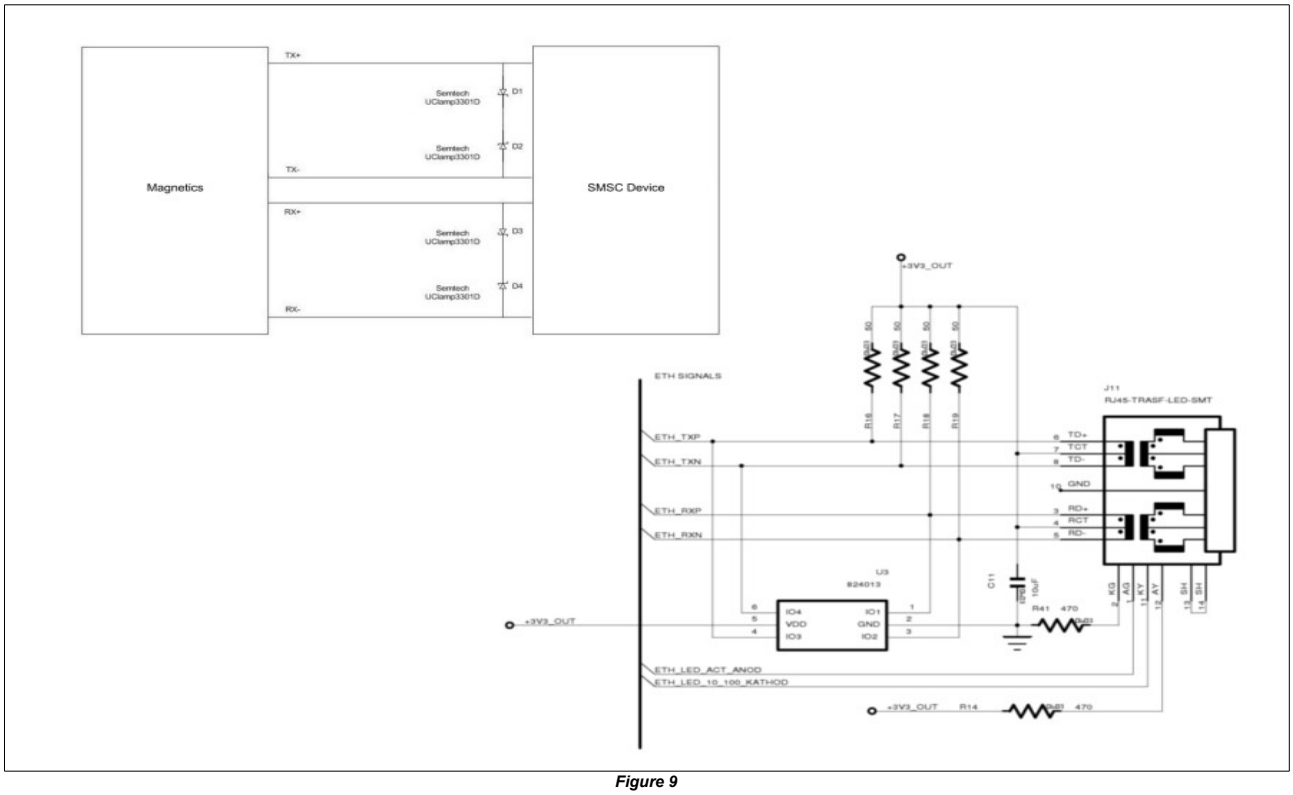


*Figure 9*

Recommended by ENGICAM:

Diode array TVS, 4 CH, ESD, 3.3V Wurth Elektronik 824013

**Note:** *for further details about PHY Protection please reffers to file AN1718 of SMSC*

## 5.7 USB interface

### 5.7.1 How to connect the USB OTG interface

The NXP iMx6 USB module provides high performance USB On-The-Go (up to 480Mbps), compatible with the USB 2.0 specification. An OTG HS PHY is also integrated so no external OTG PHY is needed on the baseboard. In the figure is shown how the MINI-AB USB/OTG connector is powered and connected in the evaluation board. In the following table are listed all USB/OTG signal of mail connector.

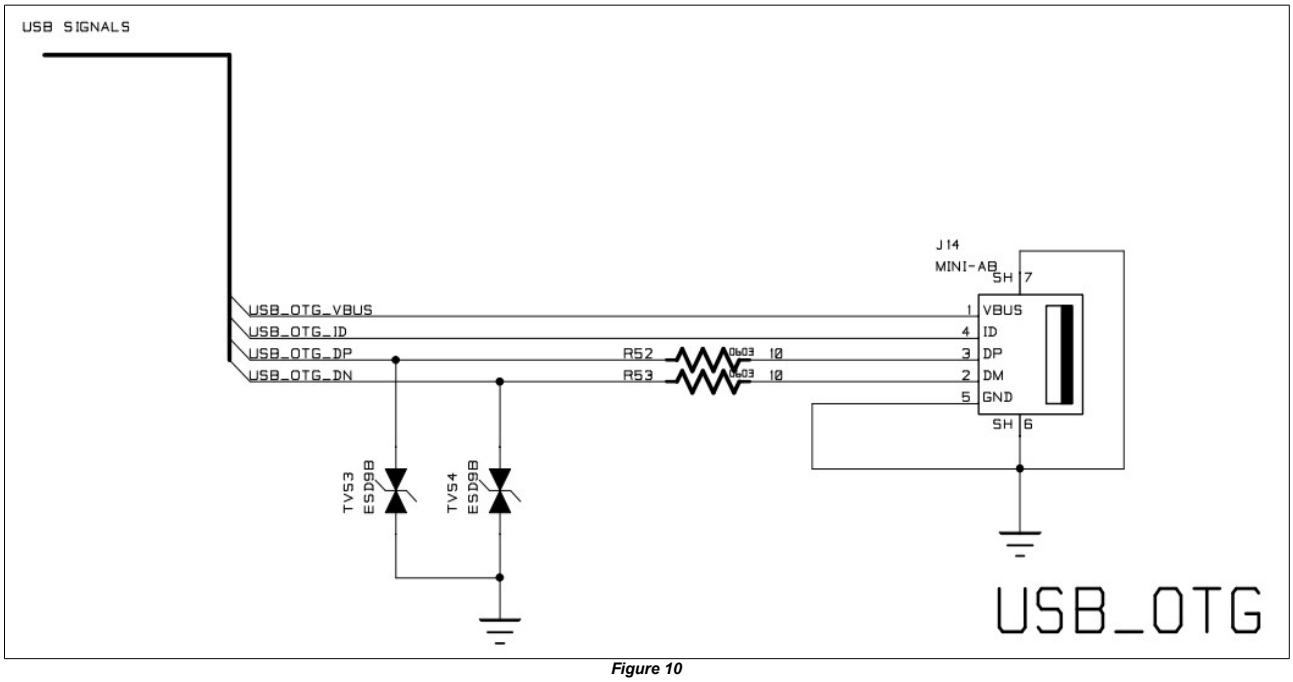


*Figure 10*

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 195 | USB_OTG_VBUS * | USB on the go interface | N | - |
| 192 | USB_OTG_DP | USB on the go interface | N | - |
| 191 | USB_OTG_ID | USB on the go interface | N | - |
| 193 | USB_OTG_DN | USB on the go interface | N | - |

*Table 15*

**** Note: The USB_OTG_VBUS is an INPUT power signal. It must be connected to 5V***

In the following figures there are shown two different ways to connect the USB OTG interface that may be used to work as either a host or a device.

Use of the USB OTG port as a Host with its own dedicated supply. The ID signal is forced to GND

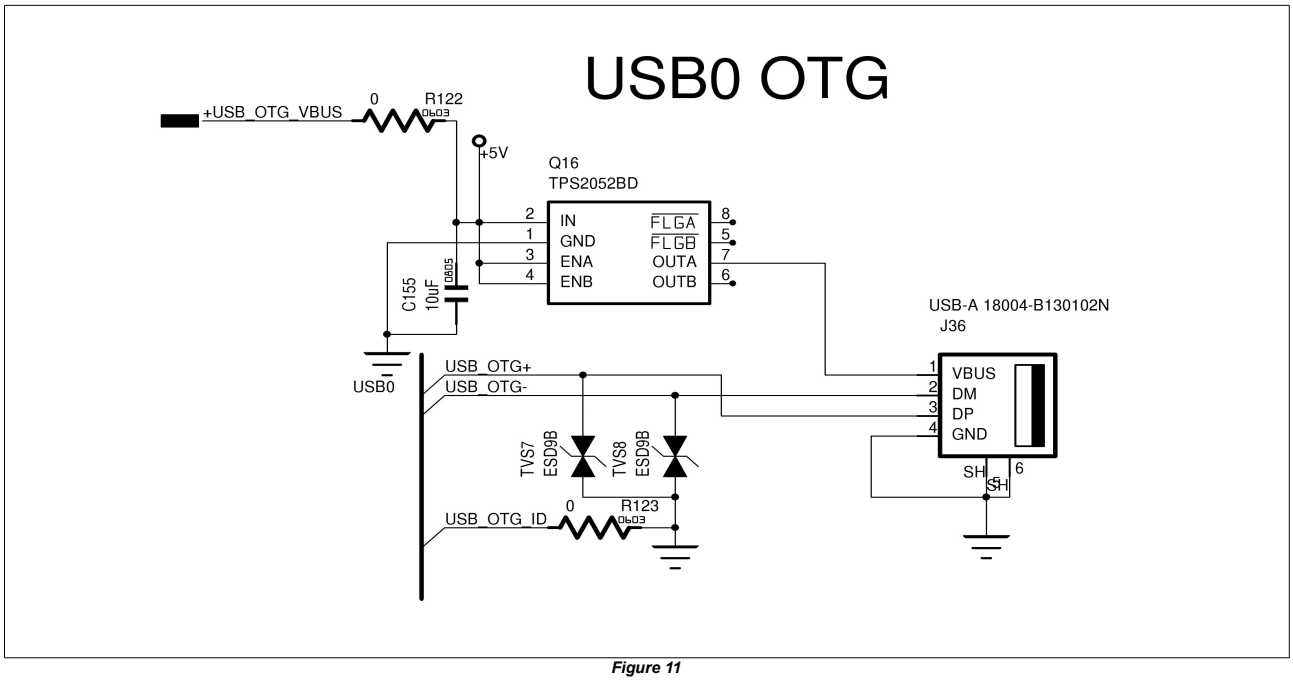


*Figure 11*

Use of the USB OTG port as Device or as Host depending on the status of the ID signal that is used also to enable the power supply.

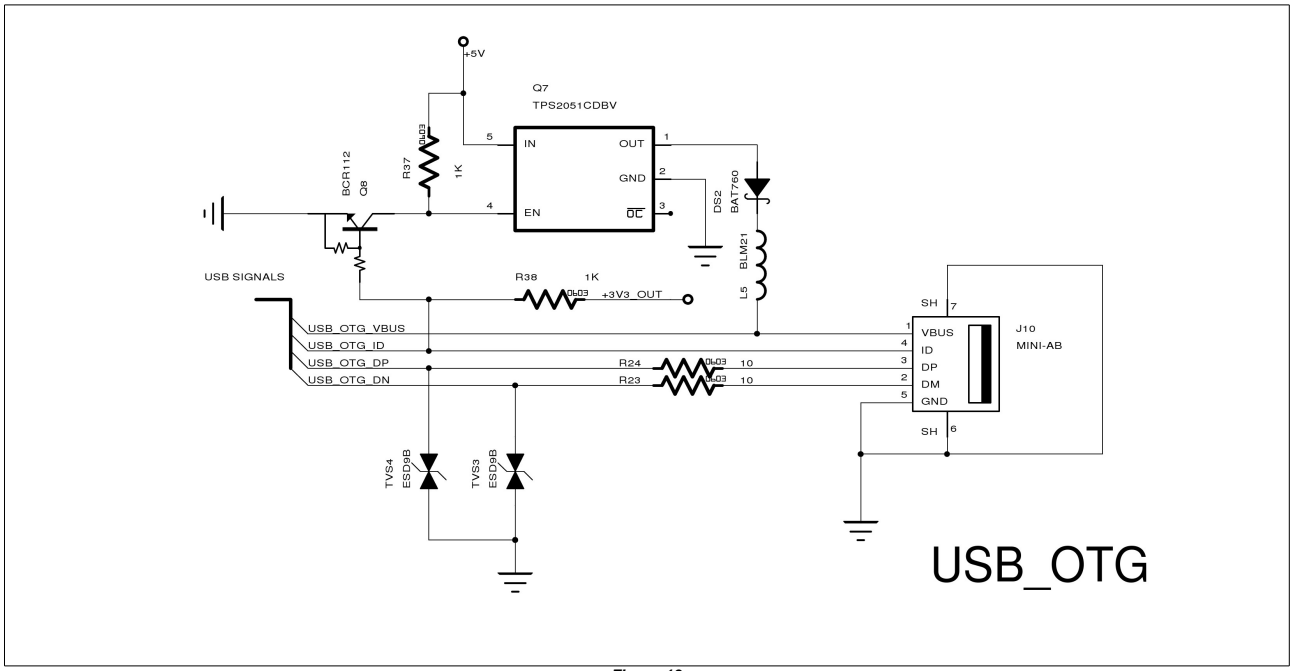


*Figure 12*

## 5.7.2 How to connect the USB host interface

The module provides one port for USB host interface. In the figure is shown how to connect this port to the Module.

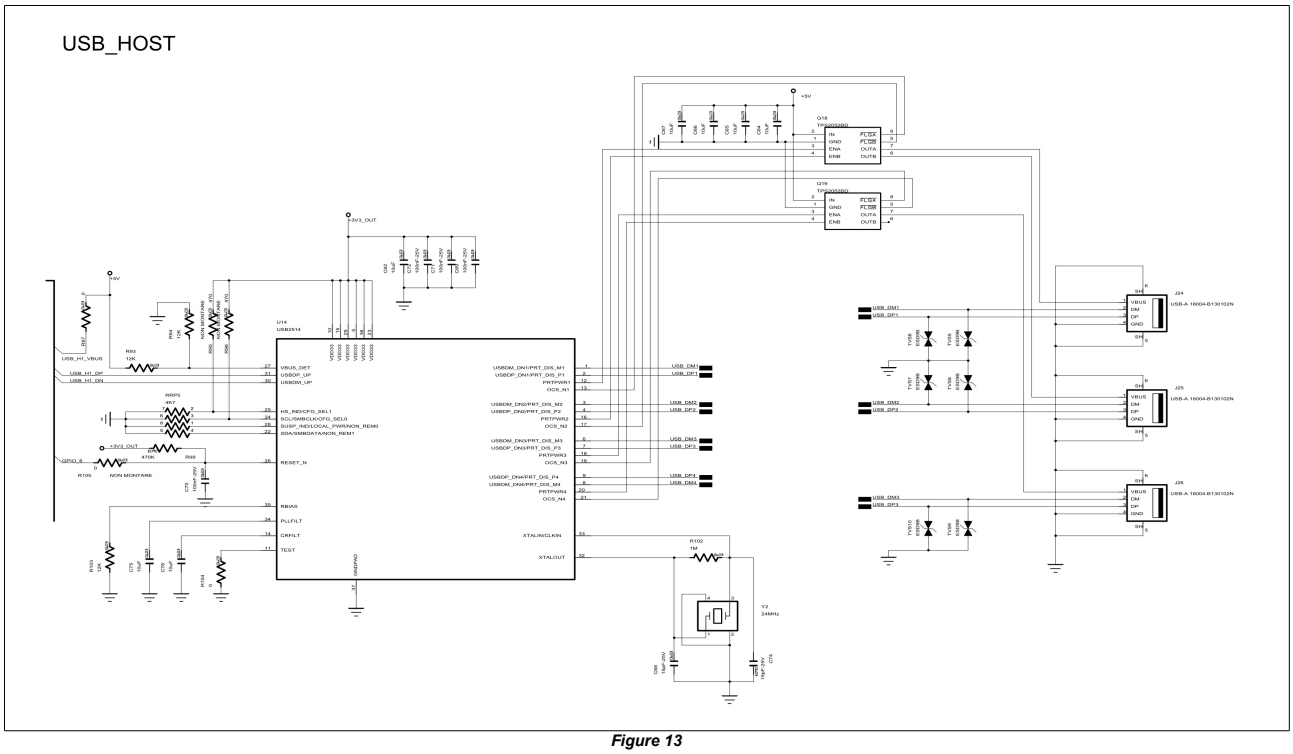


*Figure 13*

Engicam's evaluation board is equipped with an USB HUB to multiply the USB port available on module, if only one port is needed it's possible to connect it as one of the four output ports of the HUB output directly to module on pin 194-196 of the main connector.

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 180 | USB_H1_VBUS * | USB HOST interface | N | - |
| 194 | USB_HI_DP | USB HOST interface | N | - |
| 196 | USB_H1_DN | USB HOST interface | N | - |

*Table 16*

**** Note: The USB_H1_VBUS is an INPUT power signal. It must be connected to 5V***

## 5.8 How to connect the SD CARD interface

The NXP iMx6 enhanced Secured Digital Host Controller (eSDHC) provides the interface between the host system and MMC/SD/SDIO/CE-ATA cards, including cards with reduced size or mini cards. The module include this features and in the figure is shown how the Micro SD Card connector is connected to iMx6 Module in the evaluation board. The eSDHC signal of the module's main connector are listed in table below.

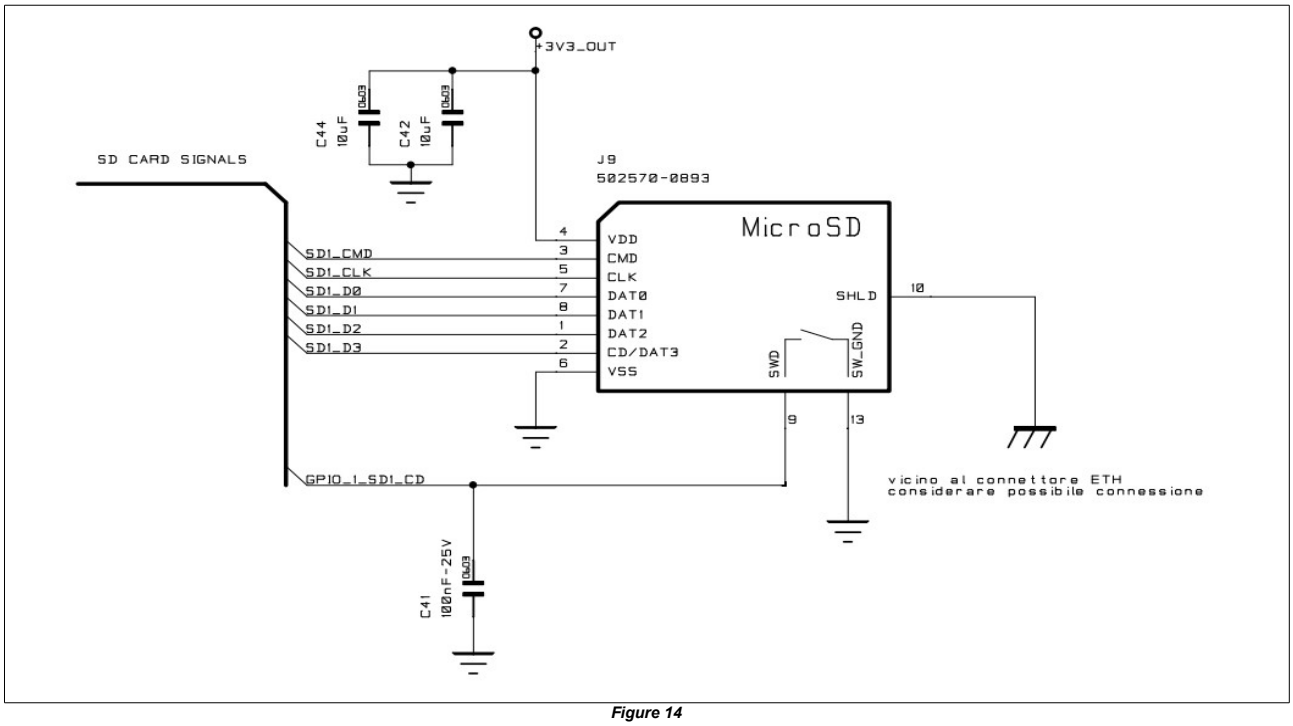


*Figure 14*

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 183 | GPIO_1_SD1_CD# | eSDHC CD Signal | Y | +3,3V |
| 184 * | GPIO_9_SD1_WP * | eSDHC WP Signal | Y | +3,3V |
| 188 | SD1_DAT0 | eSDHC DAT 0 signal | Y | +3,3V |
| 187 | SD1_DAT1 | eSDHC DAT 1 signal | Y | +3,3V |
| 185 | SD1_DAT2 | eSDHC DAT 2 signal | Y | +3,3V |
| 186 | SD1_DAT3 | eSDHC DAT 3 signal | Y | +3,3V |
| 189 | SD1_CLK | eSDHC CLK signal | Y | +3,3V |
| 190 | SD1_CMD | eSDHC CMD signal | Y | +3,3V |
| | | | | |

*Table 17*

** **Note:** This signal in the standard BSP is used as back-light intensity regulator (PWM Output Signal)*

## 5.9 How to connect an LCD display

The evaluation board of iMx6 is equipped with one RGB data port, this interface contains RGB data of 18 bit, pixel clock.
Following are reported the schematic interface with parallel URT and the map of signals.

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 125 | DISP0_CLK | LCD interface | Y | +3,3V |
| 141 | DISP0_D17 | LCD interface | Y | +3,3V |
| 142 | DISP0_D16 | LCD interface | Y | +3,3V |
| 143 | DISP0_D15 | LCD interface | Y | +3,3V |
| 144 | DISP0_D14 | LCD interface | Y | +3,3V |
| 145 | DISP0_D13 | LCD interface | Y | +3,3V |
| 146 | DISP0_D12 | LCD interface | Y | +3,3V |
| 147 | DISP0_D11 | LCD interface | Y | +3,3V |
| 148 | DISP0_D10 | LCD interface | Y | +3,3V |
| 149 | DISP0_D9 | LCD interface | Y | +3,3V |
| 150 | DISP0_D8 | LCD interface | Y | +3,3V |
| 151 | DISP0_D7 | LCD interface | Y | +3,3V |
| 152 | DISP0_D6 | LCD interface | Y | +3,3V |
| 153 | DISP0_D5 | LCD interface | Y | +3,3V |
| 154 | DISP0_D4 | LCD interface | Y | +3,3V |
| 155 | DISP0_D3 | LCD interface | Y | +3,3V |
| 157 | DISP0_D2 | LCD interface | Y | +3,3V |
| 158 | DISP0_D1 | LCD interface | Y | +3,3V |
| 159 | DISP0_D0 | LCD interface | Y | +3,3V |
| 160 | DISP0_VSYNC | LCD interface | Y | +3,3V |
| 161 | DISP0_HSYNC | LCD interface | Y | +3,3V |
| 162 | DISP0_DRDY | LCD interface | Y | +3,3V |

*Table 18*

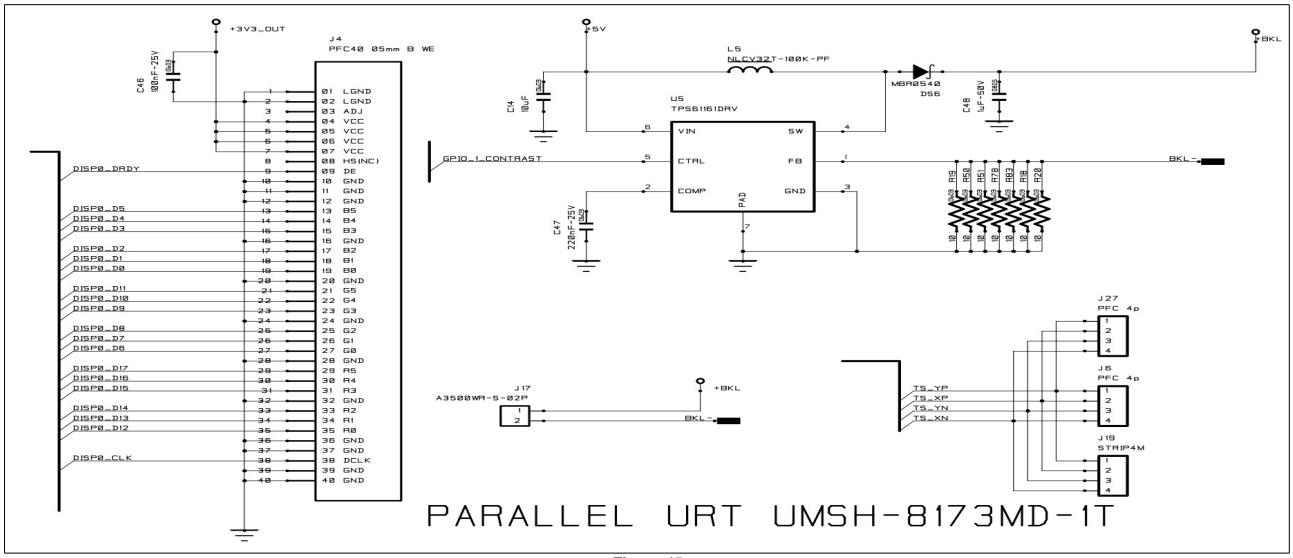


*Figure 15*

### 5.9.1 Connection map for 18 bit TFT only

The following map represent the connection mode applied to 18 bit TFT display
For every connection the colour controlled is joined

| Number | Name | 18 bit TFT connections |
|---|---|---|
| 159 | DISP0_D0 | BLU 0 |
| 158 | DISP0_D1 | BLU 1 |
| 157 | DISP0_D2 | BLU 2 |
| 155 | DISP0_D3 | BLU 3 |
| 154 | DISP0_D4 | BLU 4 |
| 153 | DISP0_D5 | BLU 5 |
| 152 | DISP0_D6 | GREEN 0 |
| 151 | DISP0_D7 | GREEN 1 |
| 150 | DISP0_D8 | GREEN 2 |
| 149 | DISP0_D9 | GREEN 3 |
| 148 | DISP0_D10 | GREEN 4 |
| 147 | DISP0_D11 | GREEN 5 |
| 146 | DISP0_D12 | RED 0 |
| 145 | DISP0_D13 | RED 1 |
| 144 | DISP0_D14 | RED 2 |
| 143 | DISP0_D15 | RED 3 |
| 142 | DISP0_D16 | RED 4 |
| 141 | DISP0_D17 | RED 5 |

*Table 19*

## 5.9.2 LVDS Interfaces

In the evaluation board there are two connections to displays with LVDS interface, each connection of 18 bit data. The LVDS ports may be used as follows:

- One single-channel output
- One dual channel output: single input, split to two output channels
- Two identical outputs: single input sent to both output channels
- Two independent outputs: two inputs sent, each, to a different output channel

Following the LVDS interfaces maps and schemes

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 42 | LVDS0_TX3_P | LVDS Interface's Signals | N | +2V5 |
| 44 | LVDS0_TX3_N | LVDS Interface's Signals | N | +2V5 |
| 46 | LVDS0_CLK_P | LVDS Interface's Signals | N | +2V5 |
| 48 | LVDS0_CLK_N | LVDS Interface's Signals | N | +2V5 |
| 50 | LVDS0_TX1_P | LVDS Interface's Signals | N | +2V5 |
| 52 | LVDS0_TX1_N | LVDS Interface's Signals | N | +2V5 |
| 58 | LVDS0_TX2_P | LVDS Interface's Signals | N | +2V5 |
| 59 | LVDS0_TX0_P | LVDS Interface's Signals | N | +2V5 |
| 60 | LVDS0_TX2_N | LVDS Interface's Signals | N | +2V5 |
| 61 | LVDS0_TX0_N | LVDS Interface's Signals | N | +2V5 |

*Table 20*

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 41 | LVDS1_TX2_N | LVDS Interface's Signals | N | +2V5 |
| 43 | LVDS1_TX2_P | LVDS Interface's Signals | N | +2V5 |
| 47 | LVDS1_TX3_N | LVDS Interface's Signals | N | +2V5 |
| 49 | LVDS1_TX3_P | LVDS Interface's Signals | N | +2V5 |
| 51 | LVDS1_TX1_N | LVDS Interface's Signals | N | +2V5 |
| 53 | LVDS1_TX1_P | LVDS Interface's Signals | N | +2V5 |
| 54 | LVDS1_TX0_N | LVDS Interface's Signals | N | +2V5 |
| 55 | LVDS1_CLK_N | LVDS Interface's Signals | N | +2V5 |
| 56 | LVDS1_TX0_P | LVDS Interface's Signals | N | +2V5 |
| 57 | LVDS1_CLK_P | LVDS Interface's Signals | N | +2V5 |

*Table 21*

In the figure below is shown LVDS ports. The not mount resistors is needed to drive TFT with only 3 LVDS “channel” this means drive TFT at 18 bit instead of 24 bit. We will refer to the channel by referring to the pair signal “P” & “N”.

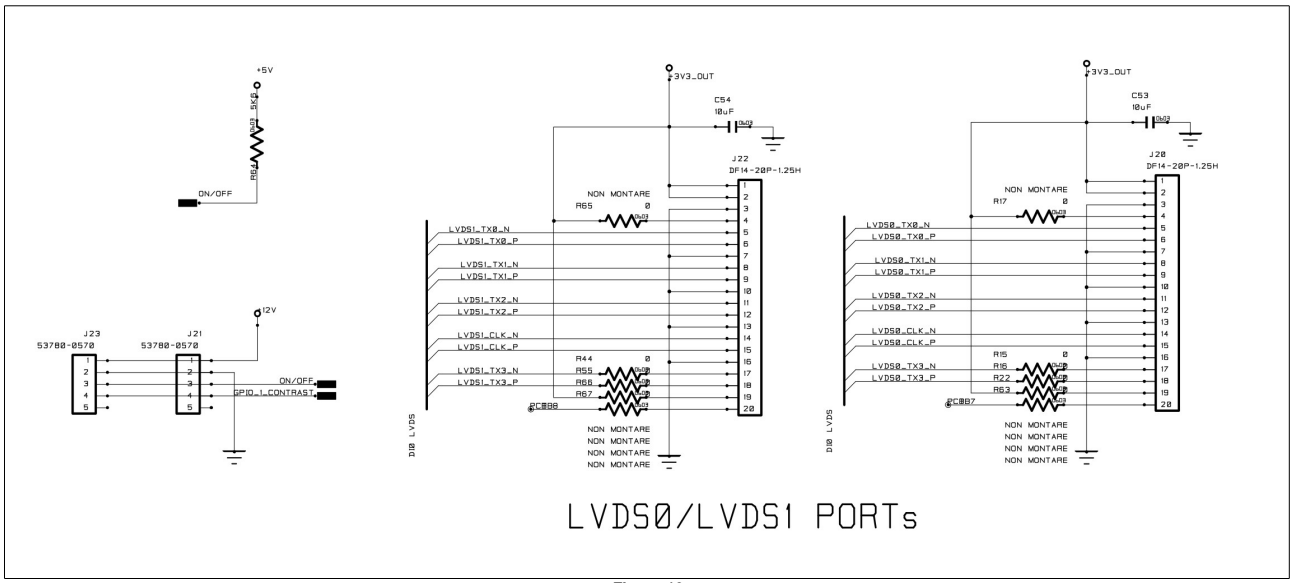


***Figure 16***

## 5.9.3 LVDS Routing and Placement Considerations

The LVDS lines are high-speed signals and as such during the designing must be complied with standards of protection against noise and crosstalk. In this chapter we give some advices about positioning, cabling and routing; for further details please follow the guidelines and the manuals about LVDS bus.
Differential line: as mentioned we are working with fast signals, then to avoid disturbances and reduce noise on the line we suggest to route the channel lines in differential mode, for the same reason also the “channel” on the cable used to connect the board to TFT should be twisted.
Distance: there is no distance recommended between the devices but, always considering the nature of signals and that the driver is the same processor iMx6, we suggest to positioning the connector as close as possible to the module, and also to be aware to matching the line of differential pair as best as you can to avoid any kind of delay.
Controlled Impedance: all the signal's pairs must be traced in controlled impedance referred to the GND plane. This should avoid the problems due to reflections on the line. We suggest that the traces for LVDS signals should be closely-coupled and designed for 100Ω differential impedance.

**Note: for further informations consult differential micro-strips and high speed routing documentations**

## 5.9.4 HDMI Interfaces

HDMI is capable of transferring uncompressed video, audio, and data using a single cable. The video pixel rates are typically from 25 MHz up to 297 MHz (4k x 2k and 3D video modes), but HDMI can support higher rates up to 340 MHz. It can support S/PDIF (IEC60958 L-PCM and IEC61937 compressed non-linear PCM: AC-3, MPEG-1/-2 Audio, DTS®, MPEG-2/-4 AAC, ATRAC, WMA, MAT) and Parallel HBR (high bit rate) audio interface, enabling the support of Dolby® True-HD and DTS-HD Master Audio. HDMI has the capability of automatically setting the display format configuration (intelligent link).

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 70 | HDMI_HPD | HDMI_HPD | N | - |
| 73 | HDMI_CECIN | HDMI_CECIN | N | - |
| 75 | HDMI_CLKM | HDMI_CLKM | N | - |
| 77 | HDMI_CLKP | HDMI_CLKP | N | - |
| 81 | HDMI_D0M | HDMI_D0M | N | - |
| 83 | HDMI_D0P | HDMI_D0P | N | - |
| 85 | HDMI_D1M | HDMI_D1M | N | - |
| 87 | HDMI_D1P | HDMI_D1P | N | - |
| 91 | HDMI_D2M | HDMI_D2M | N | - |
| 93 | HDMI_D2P | HDMI_D2P | N | - |

*Table 22*

The HDMI video out interface is implemented as shown in the figure below and using the signals shown in the table.

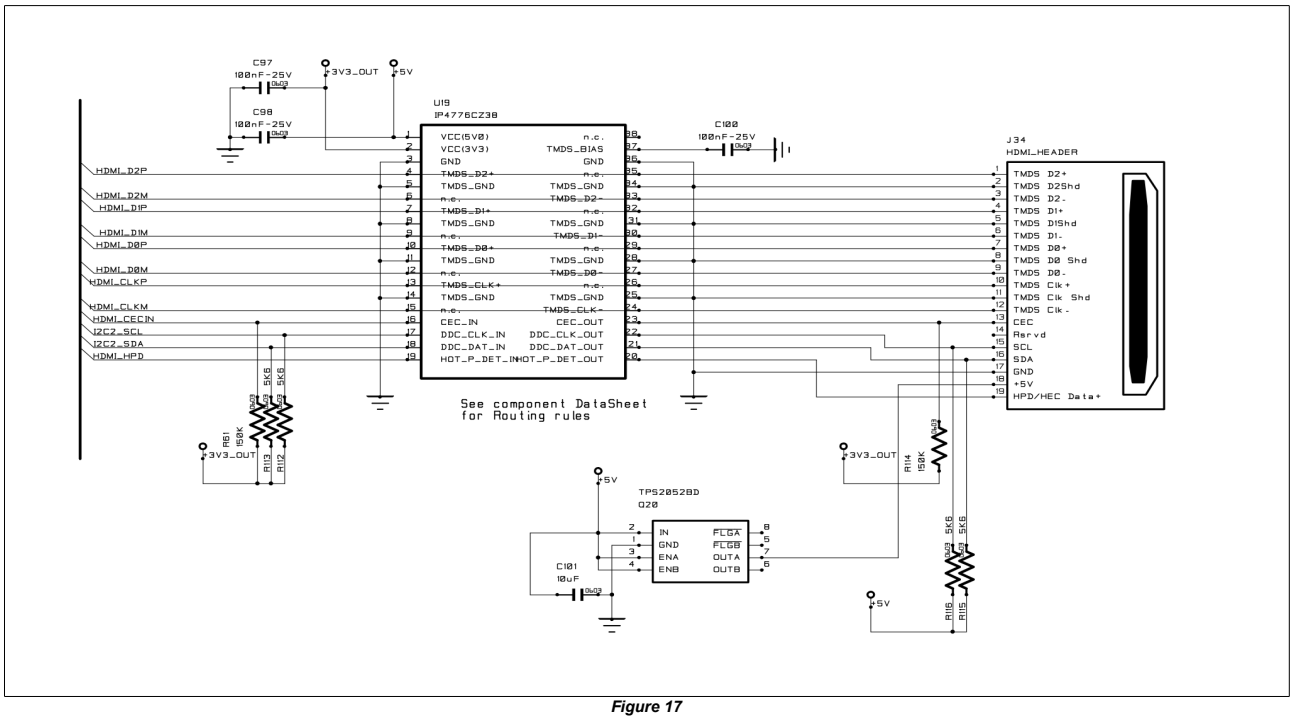


*Figure 17*

**Note:** For further details and applications please refer to iMx6RM document

## 5.10 How to connect the SATA interface

### (Only for i.CoreM6Q/i.CoreM6D)

Serial ATA (SATA or Serial Advanced Technology Attachment) is a computer bus interface for connecting host bus adapters to mass storage device such as HDD and optical drivers. Serial ATA was designed to replace the older ATA standard (also known as EIDE), offering several advantages over the older parallel ATA (PATA) interface: reduced cable-bulk and cost, native hot swapping, faster data transfer; through higher signalling rates, and more efficient transfer through an (optional) I/O queuing protocol. SATA host-adapters and devices communicate via a high-speed serial cable over two pairs of conductors. To ensure backward compatibility with legacy ATA software and applications, SATA uses the same basic ATA and ATAPI command-set as legacy ATA devices.

The iMx6 module provides a SATA II HDD interface (3.0 Gbps) includes the SATA controller and the PHY. It is a complete mixed-signal IP solution for SATA HDD connectivity. Following are reported the schematic interface and the map of signals.

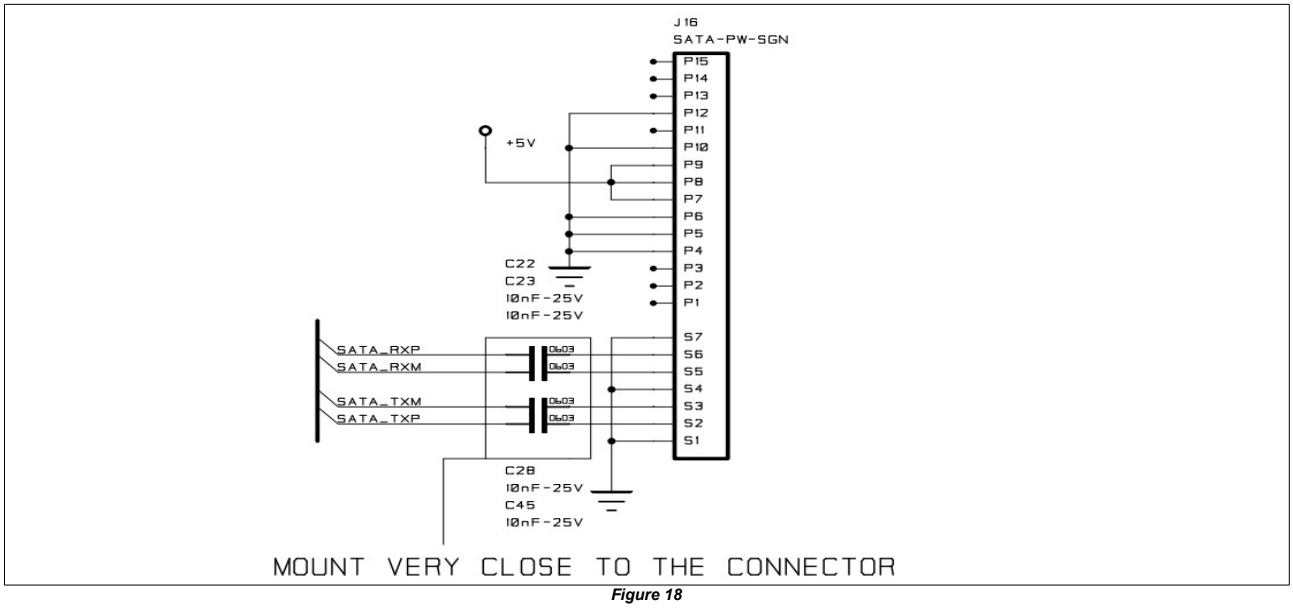


*Figure 18*

It's strongly recommended to positioning the capacitor of SATA signals as close as possible to the connector

- Transmit a 3.0 Gb/sec differential NRZ serial stream at specified voltage levels
- Provide a 100 Ohm matched termination (differential) at the transmitter
- Receive a 3.0 Gb/sec differential NRZ serial stream
- Provide a 100 Ohm matched termination (differential) at the receiver

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 101 | SATA_RXM | SATA Interface | N | - |
| 102 | SATA_TXP | SATA Interface | N | - |
| 103 | SATA_RXP | SATA Interface | N | - |
| 104 | SATA_TXM | SATA Interface | N | - |

*Table 23*

**Note:** *for further details refer to SATA specifications on **iMx6RM** document.*

## 5.11 How to connect the PCIe interface

PCIe 2.0 PHY is a complete mixed-signal semiconductor intellectual property (IP) solution, designed for single-chip integration into computer applications. The PCIe2 PHY ssp_x1 includes all the necessary logical, geometric and physical design files to implement complete PCI Express 2.0 physical layer capability for 5Gb/s operation, connecting a host controller or device controller to a PCI Express system. This product is optimized for a system-on-Chip (SoC) design targeted to the TSMC 40LP1.1/2.5-V fabrication process.

The PCIe 2.0 PHY supports both the 5 Gbp/s data rate of the PCI Express Gen 2.0 specifications as well as being backwards compatible to the 2.5Gb/s Gen 1.1 specification.

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 67 | PCIe_RXM | PCIe_RXM | N | - |
| 69 | PCIe_RXP | PCIe_RXP | N | - |
| 72 | PCIe_TXM | PCIe_TXM | N | - |
| 74 | PCIe_TXP | PCIe_TXP | N | - |
| 76 | PCIe_REFCLKM | PCIe_REFCLKM | N | - |
| 78 | PCIe_REFCLKP | PCIe_REFCLKP | N | - |

*Table 24*

*It's strongly recommended to positioning the capacitor of PCIe signals as close as possible to the connector. Capacitors on RX signals may be unnecessary and replaceable with 0 Ohm resistors*

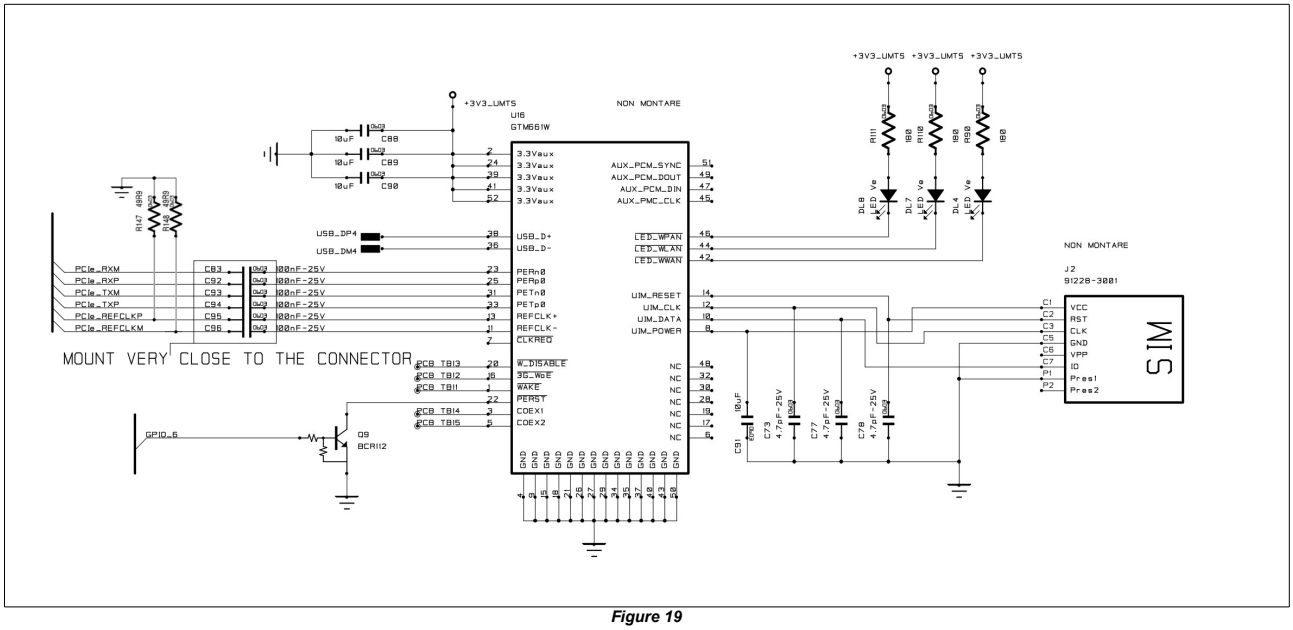


*Figure 19*

***Termination is required on the differential clock lines. Connect two 49.9 Ω resistors, one between REFCLK- and GND, the other between REFCLK+ and GND. Alternately, Connect a 100 Ω resistor between REFCLK- and REFCLK+, as close as possible to the receiver device (connector).***

***Note:*** *for further details please refer to PCIe recommendations on* ***iMx6*** *series document (as design guide* ***IMX6DQ6SDLHDG*** *and reference manual).*

## 5.12 JTAG Interface

**Joint Test Action Group** (**JTAG**) is the common name used for the IEEE 1149.1 standard entitled **Standard Test Access Port and Boundary-Scan Architecture** for test access ports used for testing printed circuit boards using boundary scan. JTAG is often used as an IC debug or probing port.

There are no official standards for JTAG adapter physical connectors. Development boards usually include a header to support preferred development tools; in some cases they include multiple such headers, because they need to support multiple such tools. For example, a micro-controller, FPGA, and ARM application processor will rarely share tools, so a development board using all of those components might have three or more headers. Production boards may omit the headers; or when space is tight, just provide JTAG signal access using test points.

In the figure below is shown how to connect a JTAG interface to iMx6 Module.

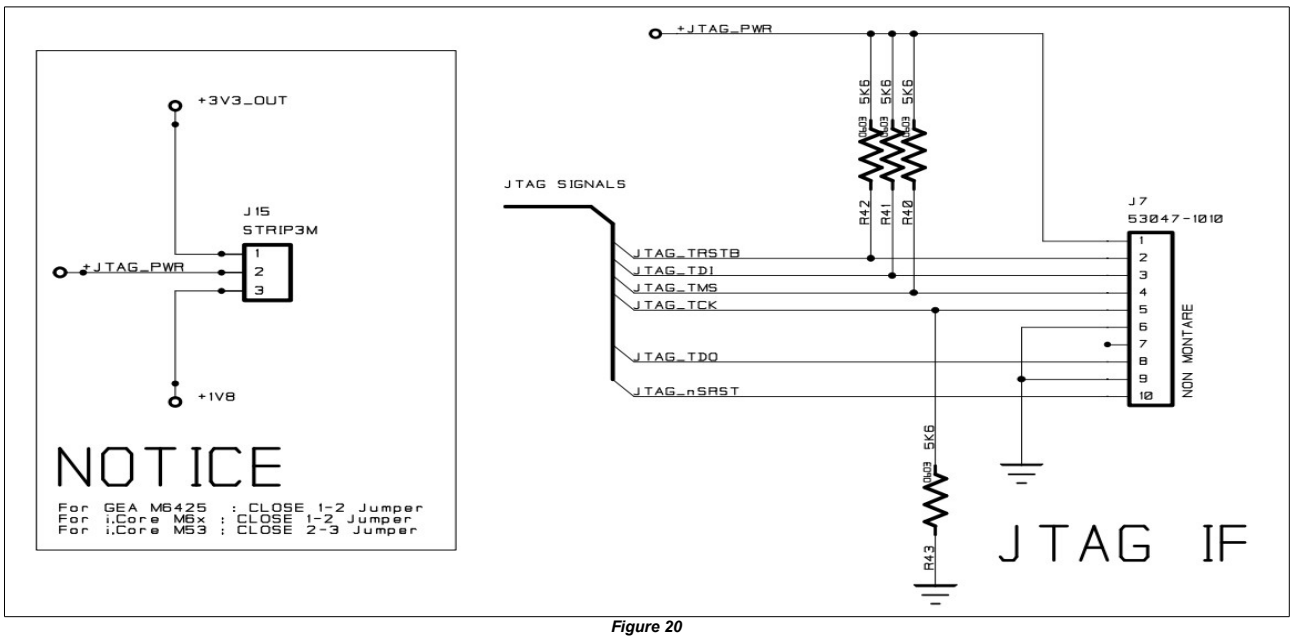


*Figure 20*

In the table are listed all JTAG signals as mapped in the main connector.

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 173 | JTAG_TRSTB | JTAG Interface | N | +3,3V |
| 174 | JTAG_TDO | JTAG Interface | N | +3,3V |
| 175 | JTAG_TDI | JTAG Interface | N | +3,3V |
| 176 | JTAG_TMS | JTAG Interface | N | +3,3V |
| 177 | JTAG_TCK | JTAG Interface | N | +3,3V |
| 179 | JTAG_nSRST | JTAG Interface with Pull-up on module | N | +3,3V |

*Table 25*

To obtain the compatibility with iMx53 Module, in the evaluation board of the iMx6 the JTAG signals are pulled up through +JTAG_PWR which could be put to +1,8V or +3,3V using jumper referenced J15.
If you intend to use both module on your main board and don't use a JTag external console is mandatory to remove the pull-up/down resistors.

***Please for further details refer to iMx6 reference manual.***

## 5.13 Boot Mode Pin

Boot mode pin determines how the module boot. The following table listed the possible options of the boot mode:

| BOOT_MODE | Action |
|---|---|
| 0 | Boot from internal modules |
| 1 | Boot from USB OTG |

*Table 26*

The boot from USB OTG is usually used for the boot loader deploy.

In the figure is shown the boot section compatible with iCoreM53 module. The closing of JM2 corresponds to put at logical 1 the boot mode pin. Also in this case to switch from iCoreM53 module to iMx6 module is necessary to use the J15 jumper to set the right value of voltage.

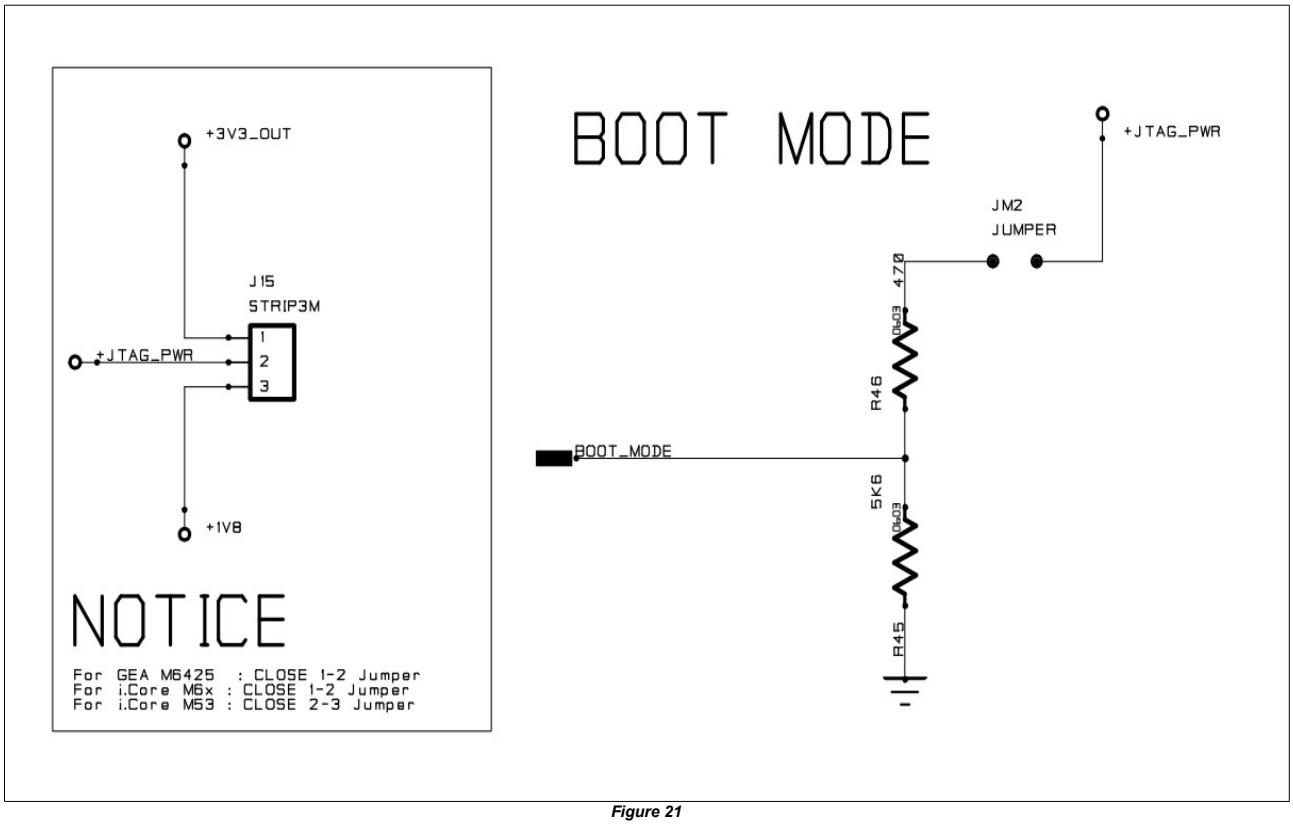


*Figure 21*

In Table below is listed the boot mode Pin numbering.

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 181 | BOOT_MODE | Boot from USB/UART or on board Nand Flash | N | - |

*Table 27*

In the evaluation board we set-up all the configurations for bootstrap from NAND and from SD card.
In the figure below is shown the boot options configurations for iMx6 on the Evaluation board.

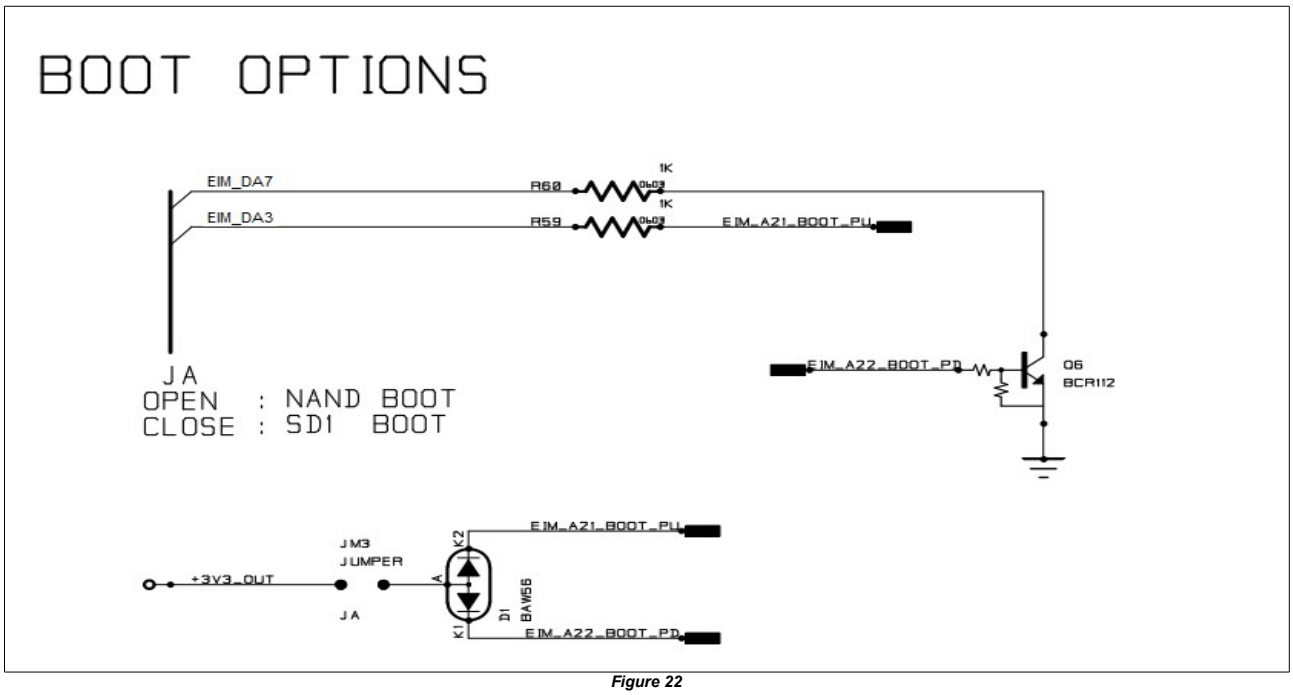


*Figure 22*

The figure above shows the implementation of the boot option applied to the EVABOARD. The signal used to configure the boot is EIM_DA7. The signal EIM_DA7 is pulled up with 12KOhm resistor.
In the standard condition the signal in the evaluation board is setting to boot from NAND Flash (jumper left open), or from SD card simply closing the jumper.
Following you can see the signals logical level to implement a custom starting sequence. The first sequence is already implemented in the module.

| BOOT FROM NAND | |
|---|---|
| **Signal** | **LOGIC LEVEL** |
| EIM_DA7 | 1 |
| EIM_DA3* | NC |

*Table 28*

The choice of boot from SD1 means short-cutting the jumper A in the evaluation board, you can have the same effect by pulling down the other signal EIM_DA7.

| BOOT FROM SD1 | |
|---|---|
| **Signal** | **LOGIC LEVEL** |
| EIM_DA7 | 0 |

*Table 29*

In the evaluation board whatever starting sequence you chose you must consider the pins 80 of main connector useful for boot configuration.

***Note: this pin is present on the EVABOARD also if is not present in the module i.CoreM6 to maintain the compatibility and the interchangeability with the other modules***

***Note: for using of any customized boot options please refer to the NXP reference manual of iMx6DQ***

### 5.13.1 Boot Signals Management

Following are shown the signals you must consider during the boot sequence:

| Signal | SODIMM Pin number | Status on Reset (*Mandatory*) | Boot Config Signal | Boot eFUSE Descriptions |
|---|---|---|---|---|
| EIM_A16 | 63 | Pull Down or Floating | BOOT_CFG3[0] | |
| EIM_A17 | 65 | Pull Down or Floating | BOOT_CFG3[1] | |
| EIM_A19 | 82 | Pull Down or Floating | BOOT_CFG3[3] | |
| EIM_A20 | 84 | Pull Down or Floating | BOOT_CFG3[4] | |
| EIM_A21 | 86 | Pull Down or Floating | BOOT_CFG3[5] | |
| EIM_A22 | 88 | Pull Down or Floating | BOOT_CFG3[6] | BT_MMU_DISABLE |
| EIM_A23 | 90 | Pull Down or Floating | BOOT_CFG3[7] | L1 I-Cache DISABLE |
| EIM_A24 | 92 | Pull Down or Floating | BOOT_CFG4[0] | |
| EIM_EB3 | 106 | Pull Down or Floating | BOOT_CFG4[7] | |

*Table 30*

The NXP documentation declares the above signals as BOOT_CFG signals but no other information (function and reset status) is currently given about them.
Basing on the Engicam test result we currently suggest to leave all these signals floating or pull down during reset status and **it's strongly recommended to consult the NXP's documentation before starting the carrier board design.**

***WARNING:***

***the table refers to the test done from the ENGICAM technicians, please always refer to the NXP's documentations to design and configure the listed BOOT_CFG signals of your own board***

## 5.14 Touch Screen Controller

Touch screen signals are implemented on MAX11801 Touch-Screen Controllers. The devices contain a 12-bit SAR ADC and a multiplexer to interface with a resistive touch-screen panel. The MAX11801's reference voltage for Touch screen signals is +3,3V

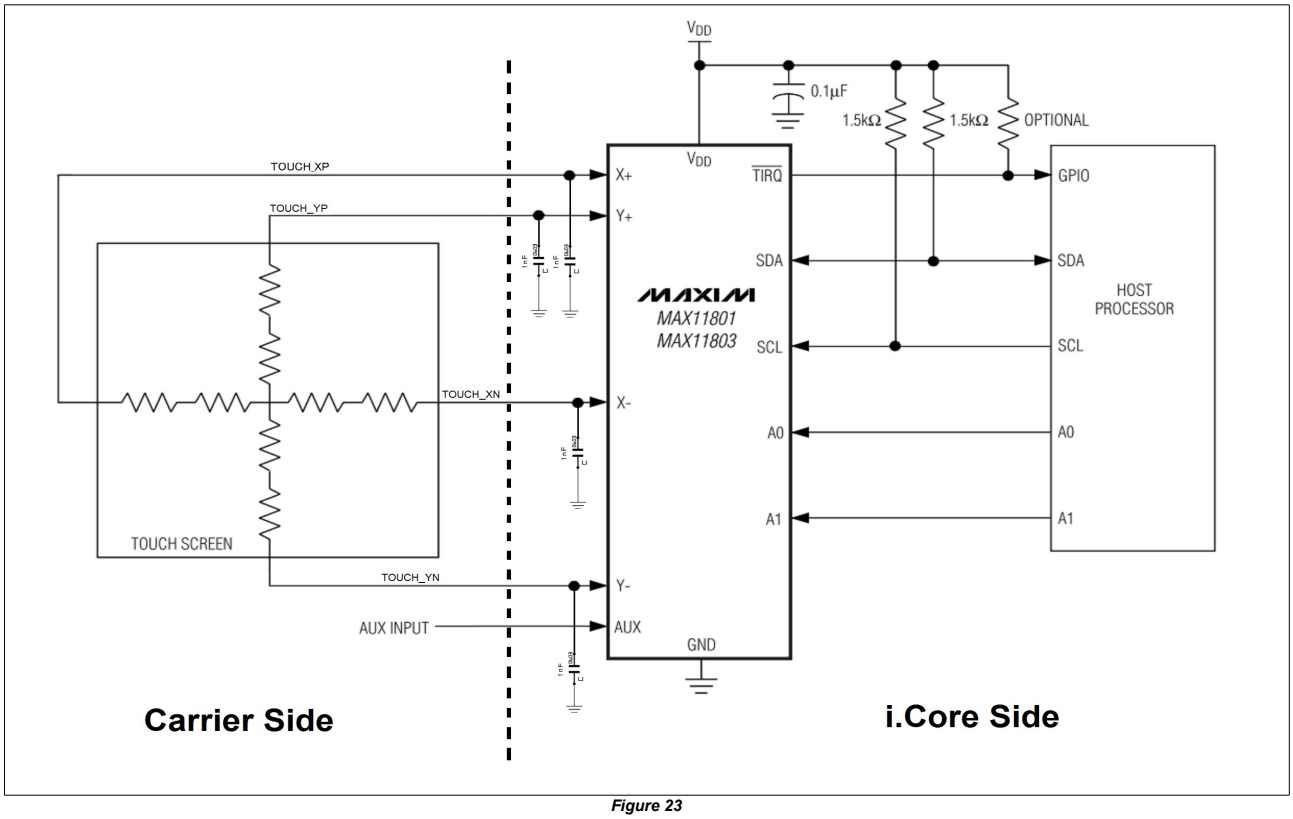


*Figure 23*

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 25 | TOUCH_XP | Touch Screen Xp | - | +3,3V |
| 26 | TOUCH_XN | Touch Screen Xn | - | +3,3V |
| 27 | TOUCH_YP | Touch Screen Yp | - | +3,3V |
| 28 | TOUCH_YN | Touch Screen Yn | - | +3,3V |

*Table 31*

***WARNING:***

Is strongly recommended to put in the carrier board's layout a ceramic capacitor per signal line (X, Y P/N) as close as possible to SODIMM connector. Through the adjust of capacitor value it's possible to improve the disturbance due to noise on X/Y signals.

*Note: A 1nF capacitor is already present on each line of the i.CoreM6 modules but it could not be enough to suppress noise.*

## 5.15 How to connect the Audio Interface

The evaluation board is equipped with the low-power stereo codec, NXP SGTL5000, that includes headphones and is designed to provide a comprehensive audio solution for portable products that require line-in, mic-in, line-out, headphone-out and digital I/O.

The figure shows how the device interface is connected to the module using the I2S BUS

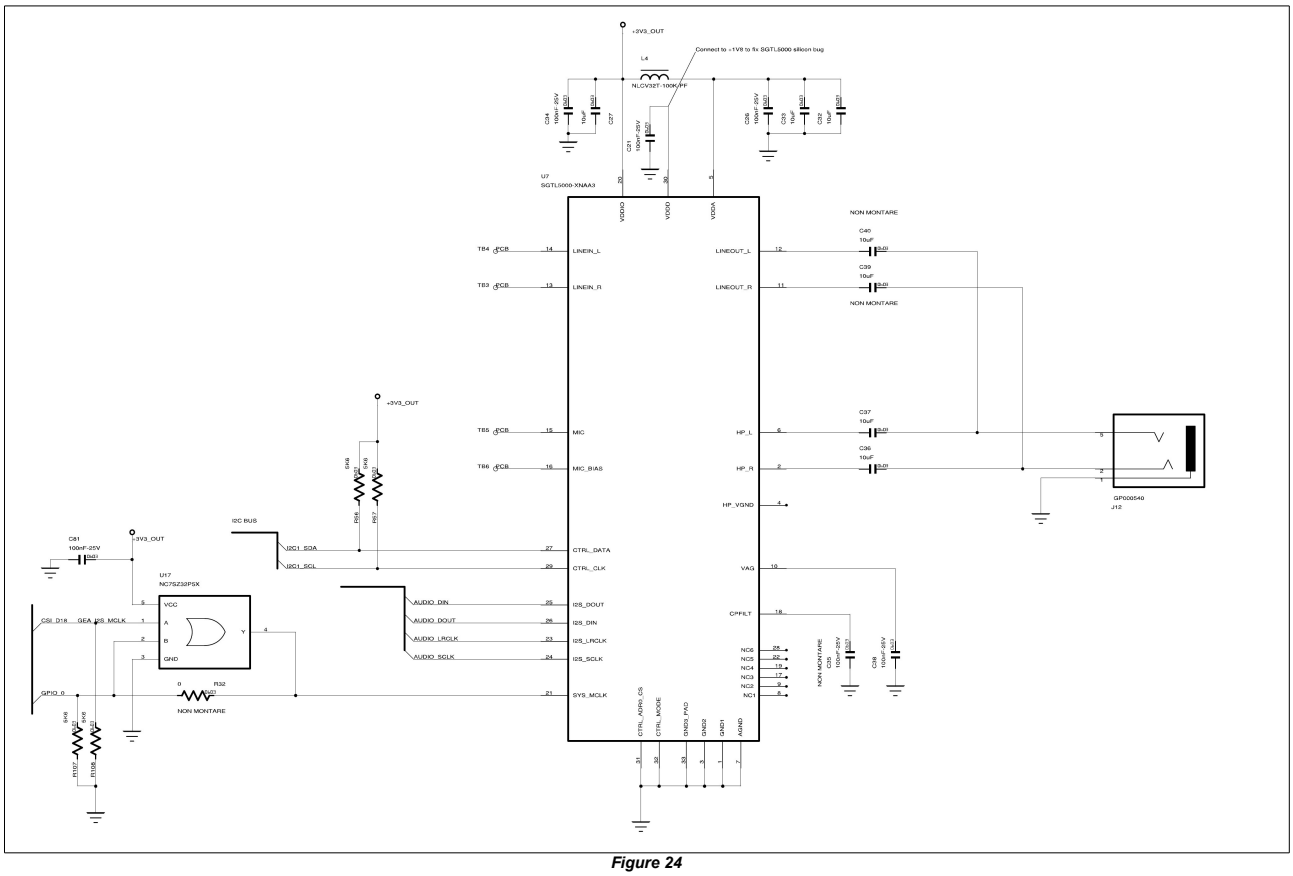


*Figure 24*

Following the I2S BUS pins numbering

| Number | Name | Primary Function Description | GPIO Capable | Voltage |
|---|---|---|---|---|
| 114 | I2S_DIN | I2S Data In | Y | +3,3V |
| 122 | I2S_DOUT | I2S_Data OUT | Y | +3,3V |
| 124 | I2S_SCLK | I2S_SCLK | Y | +3,3V |
| 115 | I2S_LRCLK | I2S_LRCLK | Y | +3,3V |

*Table 32*

**WARNING!**
**To implement the SGTL5000 on the carrier board, remember to connect the VDD, pin 30 of the SGTL5000 device, to +1V8 to fix a silicon bug (for further detail refer to SGTL5000 data sheet)**

## 5.16 How to connect the reset pin

The nRESET signal has input/output functionality and shall be driven in open-drain mode. *The signal has an internal 100K pull-up and a 100 Ohm series resistors; the maximum recommended capacitive load is about* ***100pF****.*

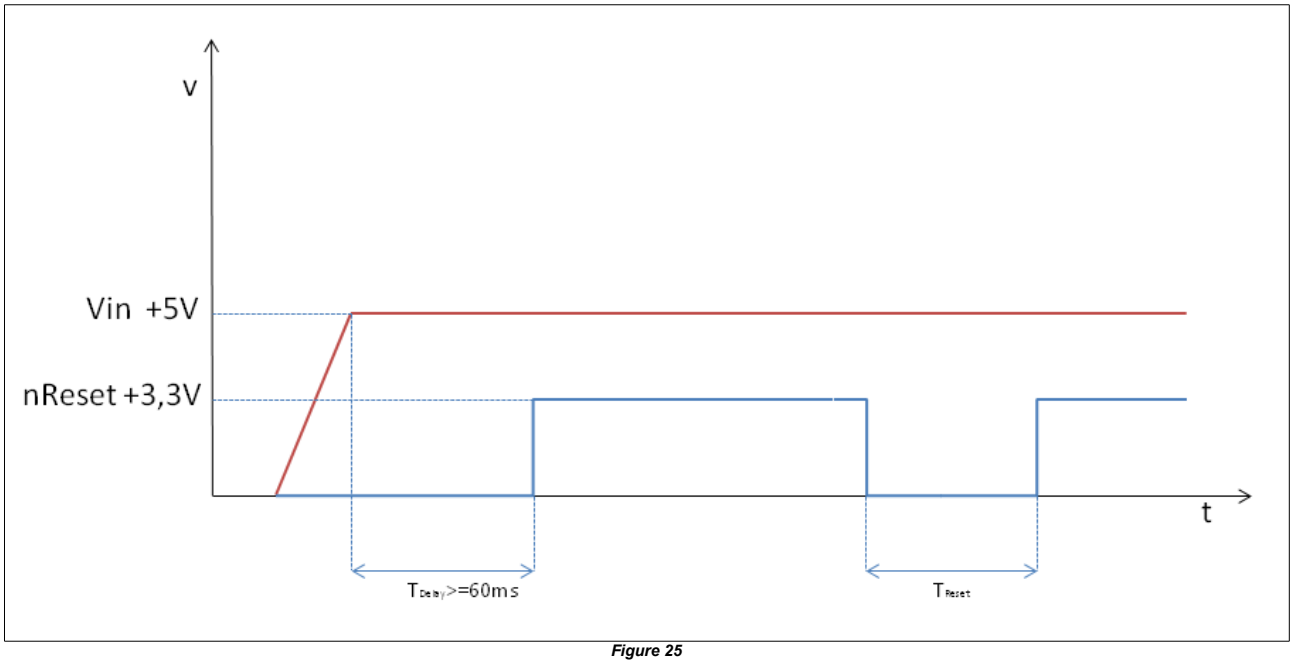


*Figure 25*

***$T_{Delay}$: driven low by SOM during the POR state***
***$T_{Reset}$: driven low by user to force POR CPU pin***

### 5.16.1 Input mode usage

The nRESET signal can be used to reset the module by driving it with an **open-drain** or with a simple button. If there are no special requirements, the module is fully auto-sufficient in terms of reset sequence, so its nRESET signal can be left floating. No Pull-up resistor is required on the carrier board; if a different pull-up resistor value (from the 100K on board of the module) is necessary, an additional pull-up on the carrier can be placed with values greater than 10K Ohm.

### 5.16.2 Output mode usage

The nRESET signal can also be used to monitor POR phase of the module, or to apply the reset (POR only) to other devices on the carrier. In this case, please take care to always respect limits imposed by maximum capacitive load and minimum additional pull-up.

***WARNING: nReset is a POR signal only, therefore it may not be driven by the SOM during another CPU reset event (e.g. WDOG reset).***

Chapter

6

# 6. Peripheral multiplexing

This Chapter gives the alternative peripheral informations

Section includes :

- ✔ **I2S**
- ✔ **SPI**
- ✔ **PWM**
- ✔ **GPT and I2C**
- ✔ **UART**
- ✔ **CSI**

## 6.1 Peripheral multiplexing description

Following we describe opportunity to use alternative interfaces using the properties of multiplexing pin.
**Please refer to the NXP's reference manual and documentation for further details (document name iMx6RM).**

### 6.1.1 SPI & IIS Configuration

Using pin multiplexing 's features we may have the following SPI and IIS connections. In the tables below are shown the output signals on the Connector's module.

ECSPI1 signals interfaces +3,3V

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 24 / 62 / 117 | EIM_D18 / CSI0_DAT5 / KEY_ROW0 | MOSI | +3,3V |
| 11 / 66 / 115 | CSI0_DAT17 / CSI0_DAT6 / DISP0_DAT22 | MISO | +3,3V |
| 94 / 124 / 130 / 116 | EIM_D16 / DISP0_DAT20 / KEY_COL0 / CSI0_DAT4 | SCK | +3,3V |
| 68 / 114 | CSI0_DAT7 / DISP0_DAT23 | SS0 | +3,3V |
| 118 / 143 | KEY_COL2 / DISP0_DAT15 | SS1 | +3,3V |
| 108 / 119 | EIM_D24 / KEY_ROW2 | SS2 | +3,3V |
| 109 / 111 | EIM_D25 / KEY_COL3 | SS3 | +3,3V |

*Table 33*

ECSPI3 signals interfaces +3,3V

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 158 | DISP0_DAT1 | MOSI | +3,3V |
| 157 | DISP0_DAT2 | MISO | +3,3V |
| 159 | DISP0_DAT0 | SCK | +3,3V |
| 155 | DISP0_DAT3 | SS0 | +3,3V |
| 154 | DISP0_DAT4 | SS1 | +3,3V |
| 153 | DISP0_DAT5 | SS2 | +3,3V |
| 152 | DISP0_DAT6 | SS3 | +3,3V |

*Table 34*

ECSPI5 signals interfaces (only for i.CoreM6Q/i.CoreM6D)

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 190 / 167 | SD1_CMD / SD2_ CMD | MOSI | +3,3V |
| 188 / 168 | SD1_DATA0 / SD2_DATA0 | MISO | +3,3V |
| 189 / 169 | SD1_CLK / SD2_ CLK | SCK | +3,3V |
| 187 / 171 | SD1_DATA1 / SD2_DATA1 | SS0 | +3,3V |
| 185 / 170 | SD1_DATA2 / SD2_DATA2 | SS1 | +3,3V |
| 186 | SD1_DATA3 | SS2 | +3,3V |
| 166 | SD2_DATA3 | SS3 | +3,3V |

*Table 35*

The following tables show the pin configurations for IIS Bus on module's connector.

IIS1 bus interfaces

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 114 | DISP0_DAT23 | I2S_DIN | +3,3V |
| 122 | DISP0_DAT21 | I2S_DOUT | +3,3V |
| 124 | DISP0_DAT20 | I2S_SCLK | +3,3V |
| 34 | GPIO_0 | I2S_MCLK | +3,3V |
| 115 | DISP0_DAT22 | I2S_LRCLK | +3,3V |

*Table 36*

### 6.1.2 Alternative PWM pins table

It's possible to set the pins shown in the following table as PWM signals.

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 184 | GPIO_9 | PWM-1 | +3,3V |
| 150 | DISP0_DAT8 | PWM-1 | +3,3V |
| 186 | SD1_DAT3 | PWM-1 | +3,3V |
| 149 | DISP0_DAT9 | PWM-2 | +3,3V |
| 183 | GPIO_1 | PWM-2 | +3,3V |
| 185 | SD1_DAT2 | PWM-2 | +3,3V |
| 187 | SD1_DAT1 | PWM-3 | +3,3V |
| 132 | SD4_DAT1 | PWM-3 | +3,3V |
| 190 | SD1_CMD | PWM-4 | +3,3V |

*Table 37*

### 6.1.3 General Purpose Timer (GPT)

Using pin multiplexing 's features we may have the following GPT and IIC connections. In the tables below are shown the output signals on the Connector's module.

GPT IN interfaces

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 188 | SD1_DATA0 | CAPIN1 | +3,3V |
| 187 | SD1_DATA1 | CAPIN2 | +3,3V |

*Table 38*

GPT OUT interfaces

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 190 | SD1_CMD | CMPOUT1 | +3,3V |
| 185 | SD1_DATA2 | CMPOUT2 | +3,3V |
| 186 | SD1_DATA3 | CMPOUT3 | +3,3V |

*Table 39*

GPT CLK interfaces

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 189 | SD1_CLK | CLKIN | +3,3V |

*Table 40*

### 6.1.4 IIC Configuration

IIC2 interfaces

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 111 | KEY_COL3 | SCL | +3,3V |
| 94 / 110 | EIM_D16 / KEY_ROW | SDA | +3,3V |

*Table 41*

IIC3 interfaces

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 23 / 36 | GPIO_5 / GPIO_3 | SCL | +3,3V |
| 24 / 38 | EIM_D18 / GPIO_6 | SDA | +3,3V |

*Table 42*

### 6.1.5 Alternative UART pins tables

The following tables shows an alternative UART configuration

UART2 interfaces

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 112 / 40 | EIM_D26 / GPIO_7 | UART2_TXD | +3,3V |
| 113 | EIM_D27 | UART2_RXD | +3,3V |

*Table 43*

UART3 interfaces

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 105 | EIM_D23 | UART3_CTS | +3,3V |
| 106 | EIM_EB3 | UART3_RTS | +3,3V |
| 108 | EIM_D24 | UART3_TXD | +3,3V |
| 109 | EIM_D25 | UART3_RXD | +3,3V |

*Table 44*

UART4 interfaces

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 11 | CSI0_DAT17 | UART4_CTS | +3,3V |
| 10 | CSI0_DAT16 | UART4_RTS | +3,3V |
| 6 / 116 | CSI0_DAT12 / KEY_COL0 | UART4_TXD | +3,3V |
| 7 / 117 | CSI0_DAT13 / KEY_ROW0 | UART4_RXD | +3,3V |

*Table 45*

UART5 interfaces

| Pin number | Pin Name on I.MX6Q | Signal reference | Voltage reference |
|---|---|---|---|
| 13 / 121 | CSI0_DAT19 / KEY_ROW4 | UART5_CTS | +3,3V |
| 12 / 120 | CSI0_DAT18 / KEY_COL4 | UART5_RTS | +3,3V |
| 8 | CSI0_DAT14 | UART5_TXD_MUX | +3,3V |
| 9 | CSI0_DAT15 | UART5_RXD_MUX | +3,3V |

*Table 46*

### 6.1.6 Alternative CMOS Sensor Interface

CSI1 interfaces

| Pin Number | Pin Name on I.MX6Q | Signal Name | Function Description | Voltage |
|---|---|---|---|---|
| 65 | EIM_A17 | IPU1_CSI1_D[12] | CMOS Sensor Interface Data | +3,3V |
| 113 | EIM_D27 | IPU1_CSI1_D[13] | CMOS Sensor Interface Data | +3,3V |
| 82 / 112 | EIM_A19 / EIM_D26 | IPU1_CSI1_D[14] | CMOS Sensor Interface Data | +3,3V |
| 84 | EIM_A20 | IPU1_CSI1_D[15] | CMOS Sensor Interface Data | +3,3V |
| 86 | EIM_A21 | IPU1_CSI1_D[16] | CMOS Sensor Interface Data | +3,3V |
| 88 | EIM_A22 | IPU1_CSI1_D[17] | CMOS Sensor Interface Data | +3,3V |
| 90 | EIM_A23 | IPU1_CSI1_D[18] | CMOS Sensor Interface Data | +3,3V |
| 92 | EIM_A24 | IPU1_CSI1_D[19] | CMOS Sensor Interface Data | +3,3V |
| 79 | EIM_D29 | IPU1_CSI1_VSYNC | CMOS Sensor Interface Vertical Sync | +3,3V |
| 106 | EIM_EB3 | IPU1_CSI1_HSYNC | CMOS Sensor Interface Horizontal Sync | +3,3V |
| 63 | EIM_A16 | IPU1_CSI1_CLK | CMOS Sensor Interface Pixel Clock | +3,3V |

*Table 47*