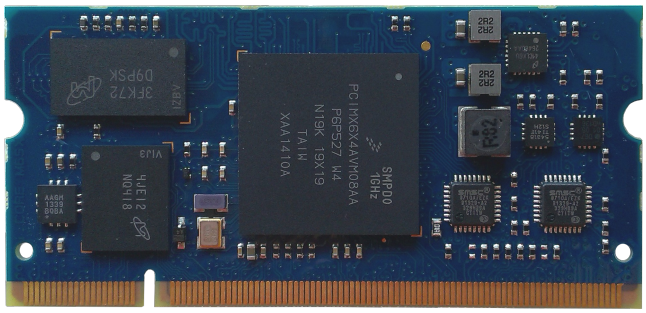
i.Core M6SX HW manual 1.0.2

Getting started manual



***** REV. 1.0.2 *****

DATE	REVISION	CHANGE DESCRIPTION
09/04/2015	1.0.0	Release
05/01/2016	1.0.1	Added Reset pin informations
16/06/2016	1.0.2	Added information for PCIe design

Summary

Chapter

1

1. Introduction

This Chapter gives background information on this document.

Section includes :

- ✔ **General Overview**
- ✔ **Acronyms and Abbreviations Used**
- ✔ **Document and Standard References**

1.1 Introduction

This document is created to guide users to design i.CoreM6SX compliant carrier board. It will focus only on the interfaces in i.CoreM6SX pinouts and related peripherals.

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

All examples of this document are based on i.Core's carrier board that is available from ENGICAM. This document also provides a collection of useful documentation, application reports, and design recommendations.

1.2 Acronyms and Abbreviations used

ABBREVIATION	EXPLANATION
ADC	Analogue to Digital Converter
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CPU	Central Processor Unit
DAC	Digital to Analogue Converter
EMI	Electromagnetic Interference, high frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
HDMI	High-Definition Multimedia Interface, combines audio and video signal
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, colour channels in common display interfaces
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
USB	Universal Serial Bus, serial interface for internal and external peripherals
NC	Not Connected pin
DNU	Do not use, leave this pin floating, not connected to the carrier
TBD	To Be Define

Table 1

1.3 Document and Standard References

1.3.1 External Industry Standard Documents

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- USB Specifications (www.usb.org).

1.3.2 NXP Documents

- i.MX6SoloXRM
- i.MX6SoloXAEC
- i.MX6SoloXCEC

Chapter

2

2. Mechanical data

This Chapter gives information about PCB and module's dimensions.

Section includes :

- ✔ **Assembly Top**
- ✔ **Assembly Bottom**
- ✔ **Mechanical dimensions**

2.1 Mechanical data

The i.MX6SoloX module has a standard SO DIMM footprint compliant with TYCO ELECTRONICS code 1473005-1 or compatible connector. The PCB dimensions is L 67.60 x W 32.1 x H 1 mm. The distances available on PCB under the module are from 1 to 1,5 mm.

2.2 Assembly Top View

The i.MX6SX Module has a Standard SODIMM footprint where odd pins are on top (component) side and even pins are on bottom side. In the Figure below is shown assembly and pin1 and pin 2 positions.

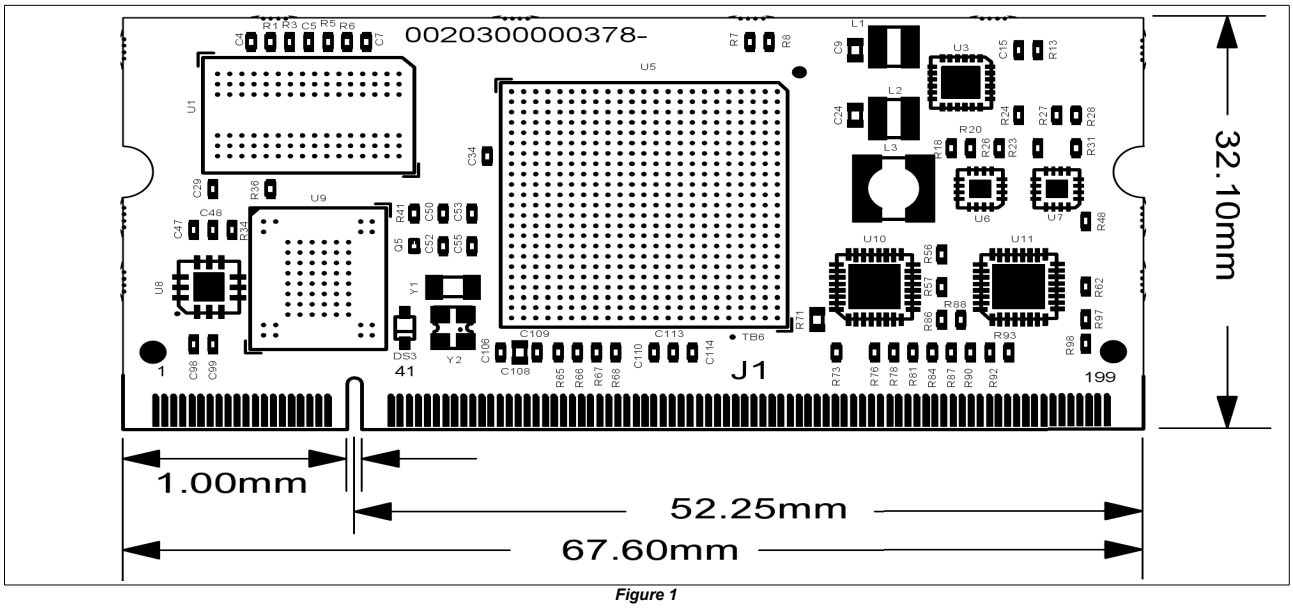


Figure 1

2.3 Assembly Bottom View

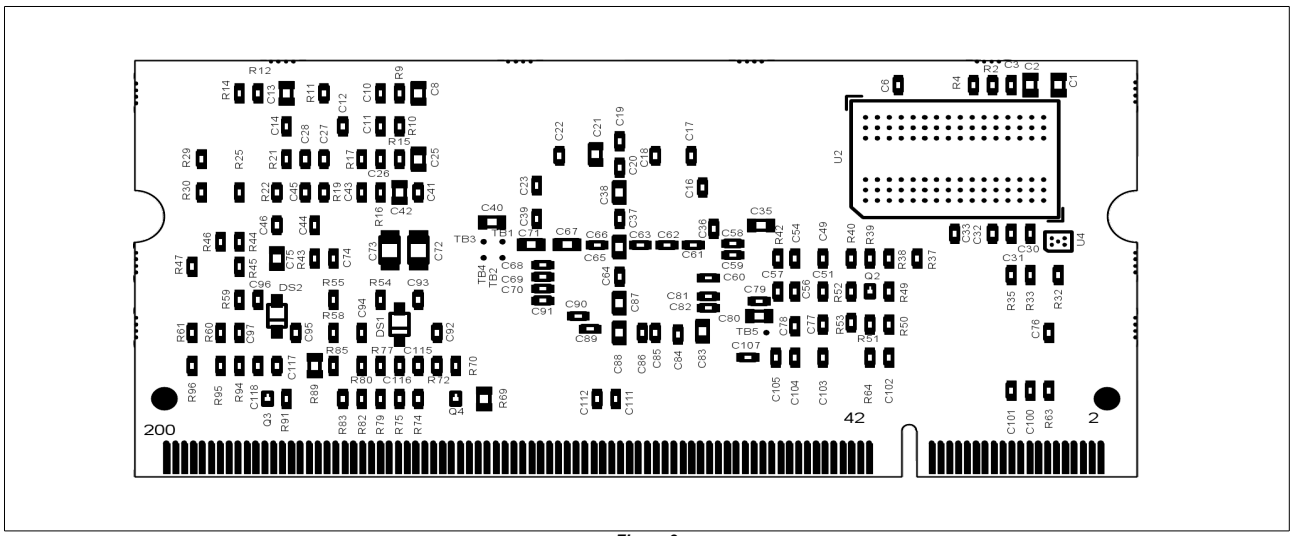


Figure 2

Chapter

3

3. Ordering Information and Features

This Chapter gives the ordering information and technical specifications of the modules.

Section includes :

- ✔ **i.CoreM6SX Ordering code**
- ✔ **Starterkit Ordering code**
- ✔ **CPU & memory specifications**
- ✔ **Operating temperature range**

3.1 Ordering Information

Following are provided the ordering informations and the description of the basic technical specifications for the modules:

Marking Code	Ordering Code	MPQ	Description	CPU & Memory specifications	Operating temperature range °C (excepted CPU)[2]	Module available at least until [1]
i.CoreM6SX	00258000010760	1	Module Sodimm i.CoreM6SX	i.MX 6 SoloX Industrial Temperature MCIMX6X4CVM08AB 800MHz core, NEON co-processor DP FPU,L1&L2 I/D cache Cortex TM -M4 @ 200 MHz core SP Floating point unit I/D cache, -40 to +105 °C [2] 32 bit Memory, temperature range industrial	-40 to +85	1"Q - 2030
i.CoreM6SX	00257000010760	58	Module Sodimm i.CoreM6SX		-40 to +85	1"Q - 2030

Table 2

Following are provided the ordering informations and the description for the module's Starterkit:

Marking Code	Ordering Code	MPQ	Description	Operating temperature range °C (excepted CPU)[2]
Starterkit i.CoreM6SX	00257000010770	1	Starterkit i.CoreM6SX 7"+ BSP/SDK Linux	-40 to +85

Table 3

[1] **Long Term Availability based on NXP longevity program**

[2] ***Note: internal junction temperature***

Chapter

4

4. Pinout

This Chapter gives the pinout informations.

Section includes :

- ✔ **Pinout overview**
- ✔ **i.MX6SoloX Pad specifications**

4.1 Module Pinout

The module's interface is achieved by a SO DIMM 200 position connector TYCO ELECTRONICS code 1473005-1 or compatible

Pin	Name	Pin Name on i.MX6SX	Primary Function Description	Type	GPIO Capable	Voltage
1	+1V8	-	Output Power PIN	O	-	-
2	+1V8	-	Output Power PIN	O	-	-
3	GND	-	Power PIN	G	N	-
4	GND	-	Power PIN	G	N	-
5	GND	-	Power PIN	G	N	-
6	CSI_DAT[00]	CSI_DATA00	CMOS Sensor Interface Data 00	I	Y	+3,3V
7	CSI_DAT[01]	CSI_DATA01	CMOS Sensor Interface Data 11	I	Y	+3,3V
8	CSI_DAT[02]	CSI_DATA02	CMOS Sensor Interface Data 02	I	Y	+3,3V
9	CSI_DAT[03]	CSI_DATA03	CMOS Sensor Interface Data 03	I	Y	+3,3V
10	CSI_DAT[04]	CSI_DATA04	CMOS Sensor Interface Data 04	I	Y	+3,3V
11	CSI_DAT[05]	CSI_DATA05	CMOS Sensor Interface Data 05	I	Y	+3,3V
12	CSI_DAT[06]	CSI_DATA06	CMOS Sensor Interface Data 06	I	Y	+3,3V
13	CSI_DAT[07]	CSI_DATA07	CMOS Sensor Interface Data 07	I	Y	+3,3V
14	CSI_VSYNC	CSI_VSYNC	CMOS Sensor Interface Vertical Sync	I	Y	+3,3V
15	CSI_HSYNC	CSI_HSYNC	CMOS Sensor Interface Horiz Sync	I	Y	+3,3V
16	CSI_CLK	CSI_PIXCLK	CMOS Sensor Interface Pixel Clock	I	Y	+3,3V
17	CSI_MCL	CSI_MCLK	CMOS Sensor Interface MCLK	O	Y	+3,3V
18	+Vcoin [2]	VDD_SNVS_IN	Backup battery or RTC	I	-	-
19	NC	-	-	-	-	-
20	NC	-	-	-	-	-
21	NC	-	-	-	-	-
22	GND	-	Power PIN	G	N	-
23	I2C1_SCL	GPIO1_IO00	I2C SCL Signal		Y	+3,3V
24	I2C1_SDA	GPIO1_IO01	I2C SDA Signal	I/O	Y	+3,3V
25	TOUCH_XP	-	Touch Screen Xp	I	-	+3,3V
26	TOUCH_XN	-	Touch Screen Xn	I	-	+3,3V
27	TOUCH_YP	-	Touch Screen Yp	I	-	+3,3V
28	TOUCH_YN	-	Touch Screen Yn	I	-	+3,3V
29	ADC1_IN0	ADC1_IN0	Analog channel 1 input 0	I	N	+3,3V
30	ADC1_IN1	ADC1_IN1	Analog channel 1 input 1	I	N	+3,3V
31	GND	-	Power PIN	G	N	-
32	ADC2_IN0	ADC2_IN0	Analog channel 2 input 0	I	N	+3,3V
33	ADC2_IN1	ADC2_IN1	Analog channel 2 input 1	I	N	+3,3V
34	AUD_MCLK	SD4_RESET_B	AUDIO_CLK_OUT	O	Y	+3,3V
35	GPIO_SP7	KEY_ROW3	Generic GPIO	I/O	Y	+3,3V
36	GPIO1_IO12	GPIO1_IO12	Generic GPIO	I/O	Y	+3,3V

Pin	Name	Pin Name on i.MX6SX	Primary Function Description	Type	GPIO Capable	Voltage
37	GPIO_SP10	SD3_CLK	Generic GPIO	I/O	Y	+3,3V
38	GPIO1_IO13	GPIO1_IO13	Generic GPIO	I/O	Y	+3,3V
39	GND	-	Power PIN	G	N	-
40	GPIO_SP4	KEY_COL2	Generic GPIO	I/O	Y	+3,3V
41	ADC1_IN2	ADC1_IN2	-	I	N	+3,3V
42	LVDS0_TX3_P	LVDS0_TX3_P	LVDS Interface's Signals	O	N	+2,5V
43	ADC1_IN3	ADC1_IN3	-	I	N	+3,3V
44	LVDS0_TX3_N	LVDS0_TX3_N	LVDS Interface's Signals	O	N	+2,5V
45	NC	-	-	-	-	-
46	LVDS0_CLK_P	LVDS0_CLK_P	LVDS Interface's Signals	O	N	+2,5V
47	ADC2_IN2	ADC2_IN2	-	I	N	+3,3V
48	LVDS0_CLK_N	LVDS0_CLK_N	LVDS Interface's Signals	O	N	+2,5V
49	ADC2_IN3	ADC2_IN3	-	I	N	+3,3V
50	LVDS0_TX1_P	LVDS0_TX1_P	LVDS Interface's Signals	O	N	+2,5V
51	GPIO_SP11	SD3_CMD	Generic GPIO	I/O	Y	+3,3V
52	LVDS0_TX1_N	LVDS0_TX1_N	LVDS Interface's Signals	O	N	+2,5V
53	GPIO_SP12	QSPI1B_SS1_B	Generic GPIO	I/O	Y	+3,3V
54	GPIO_SP13	QSPI1B_DQS	Generic GPIO	I/O	Y	+3,3V
55	GPIO_SP14	QSPI1B_DATA2	Generic GPIO	I/O	Y	+3,3V
56	GPIO_SP15	QSPI1B_DATA3	Generic GPIO	I/O	Y	+3,3V
57	NC	-	-	-	-	-
58	LVDS0_TX2_P	LVDS0_TX2_P	LVDS Interface's Signals	O	N	+2,5V
59	LVDS0_TX0_P	LVDS0_TX0_P	LVDS Interface's Signals	O	N	+2,5V
60	LVDS0_TX2_N	LVDS0_TX2_N	LVDS Interface's Signals	O	N	+2,5V
61	LVDS0_TX0_N	LVDS0_TX0_N	LVDS Interface's Signals	O	N	+2,5V
62	GPIO_SP1	KEY_COL1	Generic GPIO	I/O	Y	+3,3V
63	QSPI1A_SS0 [1]	QSPI1A_SS0_B	QuadSPI Interface	O	Y	+3,3V
64	GND	-	Power PIN	G	N	-
65	QSPI1A_SS1 [1]	QSPI1A_SS1_B	QuadSPI Interface	O	Y	+3,3V
66	GPIO_SP2	KEY_ROW0	GPIO Spare	I/O	Y	+3,3V
67	PCIe_RXM	PCIe_RXM	PCIe Interface	I	N	+2,5V
68	GPIO_SP3	KEY_ROW1	GPIO Spare	I/O	Y	+3,3V
69	PCIe_RXP	PCIe_RXP	PCIe Interface	I	N	+2,5V
70	GPIO_SP9	GPIO1_IO09	GPIO Spare	I/O	Y	+3,3V
71	GND	-	Power PIN	G	N	-
72	PCIe_TXM	PCIe_TXM	PCIe Interface	O	N	+2,5V
73	GPIO_SP8	GPIO1_IO08	GPIO Spare	I/O	Y	+3,3V
74	PCIe_TXP	PCIe_TXP	PCIe Interface	O	N	+2,5V
75	NC	-	-	-	-	-
76	PCIe_REFCLKM	CCM_CLK1_N	PCIe Interface	O	N	+2,5V

Pin	Name	Pin Name on i.MX6SX	Primary Function Description	Type	GPIO Capable	Voltage
77	NC	-	-	-	-	-
78	PCIe_REFCLKP	CCM_CLK1_P	PCIe Interface	O	N	+2,5V
79	GPIO_SP6	KEY_ROW2	GPIO Spare	I/O	-	+3,3V
80	nSD_BOOT [1]	-	-	I	N	-
81	NC	-	-	-	-	-
82	QSPI1A_SCLK	QSPI1A_SCLK	QuadSPI Interface	O	Y	+3,3V
83	NC	-	-	-	-	-
84	QSPI1A_DQS	QSPI1A_DQS	QuadSPI Interface	I	Y	+3,3V
85	NC	-	-	-	-	-
86	QSPI1A_DATA0	QSPI1A_DATA0	QuadSPI Interface	I/O	Y	+3,3V
87	NC	-	-	-	-	-
88	QSPI1A_DATA1	QSPI1A_DATA1	QuadSPI Interface	I/O	Y	+3,3V
89	GND	-	Power PIN	G	N	-
90	QSPI1A_DATA2	QSPI1A_DATA2	QuadSPI Interface	I/O	Y	+3,3V
91	NC	-	-	-	-	-
92	QSPI1A_DATA3	QSPI1A_DATA3	QuadSPI Interface	I/O	Y	+3,3V
93	NC	-	-	-	-	-
94	ETH1_TXP	-	-	O	N	-
95	GPIO_SP5	KEY_COL3	GPIO Spare	I/O	Y	+3,3V
96	ETH1_TXN	-	-	O	-	-
97	ETH1_LED_10_100_KATHOD	-	-	K	N	-
98	ETH1_RXP	-	-	I	-	-
99	ETH1_LED_ACT_ANOD	-	-	A	-	-
100	ETH1_RXN	-	-	I	-	-
101	VADC_IN3	VADC_IN3	Composite video input 3	I	N	+3,3V
102	VADC_IN2	VADC_IN2	Composite video input 2	I	N	+3,3V
103	VADC_IN1	VADC_IN1	Composite video input 1	I	N	+3,3V
104	VADC_IN0	VADC_IN0	Composite video input 0	I	N	+3,3V
105	UART3_CTS	QSPI1B_DATA0	UART3 CTS signal	O	Y	+3,3V
106	UART3_RTS [1]	QSPI1B_DATA1	UART3 RTS signal	I	Y	+3,3V
107	GND	-	Power PIN	G	N	-
108	UART3_TXD	QSPI1B_SS0_B	UART3 TXD signal	O	Y	+3,3V
109	UART3_RXD	QSPI1B_SCLK	UART3 RXD signal	I	Y	+3,3V
110	I2C2_SDA	SD4_DATA2	I2C SDA Signal	I/O	Y	+3,3V
111	I2C2_SCL	SD4_DATA3	I2C SCL Signal	O	Y	+3,3V
112	UART2_TXD	GPIO1_IO06	UART2 TXD signal	O	Y	+3,3V
113	UART2_RXD	GPIO1_IO07	UART2 RXD signal	I	Y	+3,3V
114	I2S_DIN	SD3_DATA0	I2S Data In	I	Y	+3,3V
115	I2S_LRCLK	SD3_DATA2	I2S RCLK	I/O	Y	+3,3V
116	UART1_TX	GPIO1_IO04	UART1 TXD signal	O	Y	+3,3V

Pin	Name	Pin Name on i.MX6SX	Primary Function Description	Type	GPIO Capable	Voltage
117	UART1_RX	GPIO1_IO05	UART1 RXD signal	I	Y	+3,3V
118	CAN1_TX	SD3_DATA5	CAN 1 transmit signal	O	Y	+3,3V
119	CAN1_RX	SD3_DATA7	CAN 1 receive signal	I	Y	+3,3V
120	CAN2_TX	SD3_DATA6	CAN 2 transmit signal	O	Y	+3,3V
121	CAN2_RX	SD3_DATA4	CAN 2 receive signal	I	Y	+3,3V
122	I2S_DOUT	SD3_DATA3	I2S Data Out	O	Y	+3,3V
123	GND	-	Power PIN	G	N	-
124	I2S_SCLK	SD3_DATA1	I2S SCLK	I/O	Y	+3,3V
125	DISP0_CLK	LCD1_CLK	LCD interface	O	Y	+3,3V
126	NC	-	-	-	-	-
127	ETH0_TXN	-	Fast Ethernet TXN signal	O	-	-
128	nRESET	POR	Reset signal	I	N	+3,3V
129	ETH0_TXP	-	Fast Ethernet TXP signal	O	-	-
130	GPIO_SP0	KEY_COL0	GPIO Spare	O	Y	+3,3V
131	ETH0_RXN	-	Fast Ethernet RXN signal	I	-	-
132	DISP0_CONTRAST [7]	LCD1_DATA23	LCD interface	O	Y	+3,3V
133	ETH0_RXP	-	Fast Ethernet RXP signal	I	-	-
134	+3V3_OUT	-	Output Power PIN	O	N	-
135	+3V3_OUT	-	Output Power PIN	O	N	-
136	NC	-	-	-	-	-
137	ETH0_LED_10_100_KATHOD	-	Led Indicator Cathode signal	K	-	-
138	NC	-	-	-	-	-
139	ETH0_LED_ACT_ANOD	-	Led indicator Anode signal	A	-	-
140	+3V3_OUT	-	Output Power PIN	O	-	-
141	DISP0_D17 [7]	LCD1_DATA17	LCD interface	O	Y	+3,3V
142	DISP0_D16 [7]	LCD1_DATA16	LCD interface	O	Y	+3,3V
143	DISP0_D15 [7]	LCD1_DATA15	LCD interface	O	Y	+3,3V
144	DISP0_D14 [7]	LCD1_DATA14	LCD interface	O	Y	+3,3V
145	DISP0_D13 [7]	LCD1_DATA13	LCD interface	O	Y	+3,3V
146	DISP0_D12 [7]	LCD1_DATA12	LCD interface	O	Y	+3,3V
147	DISP0_D11 [7]	LCD1_DATA11	LCD interface	O	Y	+3,3V
148	DISP0_D10 [7]	LCD1_DATA10	LCD interface	O	Y	+3,3V
149	DISP0_D9 [7]	LCD1_DATA9	LCD interface	O	Y	+3,3V
150	DISP0_D8 [7]	LCD1_DATA8	LCD interface	O	Y	+3,3V
151	DISP0_D7 [7]	LCD1_DATA7	LCD interface	O	Y	+3,3V
152	DISP0_D6 [7]	LCD1_DATA6	LCD interface	O	Y	+3,3V
153	DISP0_D5 [7]	LCD1_DATA5	LCD interface	O	Y	+3,3V
154	DISP0_D4 [7]	LCD1_DATA4	LCD interface	O	Y	+3,3V
155	DISP0_D3 [7]	LCD1_DATA3	LCD interface	O	Y	+3,3V
156	GND	-	Power PIN	G	N	-

Pin	Name	Pin Name on i.MX6SX	Primary Function Description	Type	GPIO Capable	Voltage
157	DISP0_D2 "	LCD1_DATA2	LCD interface	O	Y	+3,3V
158	DISP0_D1 "	LCD1_DATA1	LCD interface	O	Y	+3,3V
159	DISP0_D0 "	LCD1_DATA0	LCD interface	O	Y	+3,3V
160	DISP0_VSYNC	LCD1_VSYNC	LCD interface	O	Y	+3,3V
161	DISP0_HSYNC	LCD1_HSYNC	LCD interface	O	Y	+3,3V
162	DISP0_DRDY	LCD1_ENABLE	LCD interface	O	Y	+3,3V
163	NC	-	-	-	-	-
164	NC	-	-	-	-	-
165	NC	-	-	-	-	-
166	SD2_D3	SD2_DATA3	eSDHC 2 DAT 3 signal	I/O	Y	+3,3V
167	SD2_CMD	SD2_CMD	eSDHC 2 CMD signal	O	Y	+3,3V
168	SD2_D0	SD2_DATA0	eSDHC 2 DAT 0 signal	I/O	Y	+3,3V
169	SD2_CLK	SD2_CLK	eSDHC 2 CLK signal	O	Y	+3,3V
170	SD2_D2	SD2_DATA2	eSDHC 2 DAT 2 signal	I/O	Y	+3,3V
171	SD2_D1	SD2_DATA1	eSDHC 2 DAT 1 signal	I/O	Y	+3,3V
172	NC	-	-	-	-	-
173	JTAG_TRSTB	JTAG_TRSTB	JTAG Interface	I	N	+3,3V
174	JTAG_TDO	JTAG_TDO	JTAG Interface	O	N	+3,3V
175	JTAG_TDI	JTAG_TDI	JTAG Interface	I	N	+3,3V
176	JTAG_TMS	JTAG_TMS	JTAG Interface	I	N	+3,3V
177	JTAG_TCK	JTAG_TCK	JTAG Interface	I	N	+3,3V
178	NC	-	-	-	-	-
179	JTAG_nSRST	POR	JTAG Interf. Pull-up on module	I	N	+3,3V
180	USB_H1_VBUS	USB_OTG2_VBUS	USB HOST interface	I	N	-
181	BOOT_MODE	-	Boot mode selection	I	-	-
182	GND	-	Power PIN	G	N	-
183	SD1_CD	GPIO1_IO02	eSDHC CD Signal	I	Y	+3,3V
184	GPIO1_IO11	GPIO1_IO11	Generic GPIO	I/O	Y	+3,3V
185	SD1_D2	SD1_DATA2	eSDHC DAT 2 signal	I/O	Y	+3,3V
186	SD1_D3	SD1_DATA3	eSDHC DAT 3 signal	I/O	Y	+3,3V
187	SD1_D1	SD1_DATA1	eSDHC DAT 1 signal	I/O	Y	+3,3V
188	SD1_D0	SD1_DATA0	eSDHC DAT 0 signal	I/O	Y	+3,3V
189	SD1_CLK	SD1_CLK	eSDHC CLK signal	O	Y	+3,3V
190	SD1_CMD	SD1_CMD	eSDHC CMD signal	O	Y	+3,3V
191	USB_OTG_ID	GPIO1_IO10	USB on the go interface	I	Y	+3,3V
192	USB_OTG_DP	USB_OTG1_DP	USB on the go interface	-	N	-
193	USB_OTG_DN	USB_OTG1_DN	USB on the go interface	-	N	-
194	USB_H1_DP	USB_OTG2_DP	USB HOST interface	-	N	-
195	USB_OTG_VBUS	USB_OTG1_VBUS	USB on the go interface	I	N	-
196	USB_H1_DN	USB_OTG2_DN	USB HOST interface	-	N	-

Pin	Name	Pin Name on i.MX6SX	Primary Function Description	Type	GPIO Capable	Voltage
197	+5Vin	-	Power PIN	P	N	-
198	+5Vin	-	Power PIN	P	N	-
199	+5Vin	-	Power PIN	P	N	-
200	+5Vin	-	Power PIN	P	N	-

Table 4

[1] *Note: for the use of this pin please refer to boot option in "**Boot Mode Pin"** chapter*

[2] *Connect to Coin-Cell or Super-Cap; left floating if not use*

The yellow lines highlight the required minimum electrical connections in order to make the module working correctly.

Chapter

5

5. Carrier Board Design

This Chapter gives the technical specifications for carrier board design.

Section includes :

- ✔ **Carrier Board recommendations**
- ✔ **Power signals and backup battery**
- ✔ **Serials**
- ✔ **CAN Bus**
- ✔ **Ethernet**
- ✔ **USB + USB OGT**
- ✔ **SDIO**
- ✔ **LCD and LVDS**
- ✔ **SATA**
- ✔ **PCIe**
- ✔ **Jtag interface**
- ✔ **Boot mode**
- ✔ **Touch screen controller**
- ✔ **Reset pin management**

5.1 Carrier board recommended specifications

Following we'll describe the specifications required to carrier board to avoid problems of assembly process. The module is interfaced with the carrier board through a SO-DIMM with 200 positions connector type TYCO ELECTRONICS code 1473005-1 or compatible.
For proper assembly is strongly recommended to paying attention to:

5.1.1 Planarity in finish process

Due to the technical and mechanical specifications of the connector we suggest the maximum planarity of the footprint on PCB, so we suggest a type of finish obtained by horizontal process (we suggest and use for our carrier boards a type Chemical Gold finish).

5.1.2 Planarity of PCB

Also the planarity of the entire Printed Circuit Board must be kept in check especially when the your carrier board grows in size. In this case we suggest you contact the manufacturer of PCB to understand how improve the planarity of ended board and optimize the process maintaining the electrical characteristics unchanged

Note: for further detail please refer to your SO-DIMM connector's data-sheet

5.1.3 Power Supply

It's strongly recommended that the power supply of the carrier board, which feeds the driver and control devices connected with the i.MX processor, begins to work after the initialization of the processor itself

5.2 How to power the i.MX6SX module

Please read carefully the related sections before start your power stage design. This module needs to be supply up to +5Vin power. Please refer to the table below for the power supply range specification. The power dissipated by the module in the operating mode is about 250-350 mA, but **the system must provide at least a power of 2A at 5V to allow the start of the module.**

	Min	Typ	Max
Voltage range	-	+5V	+5,5V
i.CoreM6SX Current @ 5,0V	-	480 mA	-

Table 5

Note: *the measure of table above are to be considered referred to the module with only the Linux OS running, the use of graphic accelerators or other multimedia applications could be cause of higher consumption than those indicated.*

In the following table are shown the module power supply pins numbering, please connect all power supply pins in order to avoid damage.

Number	Name	Primary Function Description	GPIO Capable	Voltage
197	+5Vin	Power PIN	N	-
198	+5Vin	Power PIN	N	-
199	+5Vin	Power PIN	N	-
200	+5Vin	Power PIN	N	-
3	GND	Power PIN	N	-
4	GND	Power PIN	N	-
5	GND	Power PIN	N	-
22	GND	Power PIN	N	-
31	GND	Power PIN	N	-
39	GND	Power PIN	N	-
64	GND	Power PIN	N	-
71	GND	Power PIN	N	-
89	GND	Power PIN	N	-
107	GND	Power PIN	N	-
123	GND	Power PIN	N	-
156	GND	Power PIN	N	-
182	GND	Power PIN	N	-

Table 6

i.MX6SX module has 5 Output power PIN usable for power source. In the table below are shown the power supply pins numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
1	+1V8	Output Power PIN	N	-
2	+1V8	Output Power PIN	N	-
134	+3V3_OUT	Output Power PIN	N	-
135	+3V3_OUT	Output Power PIN	N	-
140	+3V3_OUT	Output Power PIN	N	-

Table 7

In the following table are shown the nominal maximum rating of power output:

Power output	Max output current
+1V8	200 mA (Total)
+3V3_OUT	1000 mA (Total)

Table 8

WARNING!

The currents above 600 mA provided by the +3V3_OUT of the module, help to lower the performance in temperature.
We recommend to add a regulator voltage for an external current greater than or equal to 600 mA, in those applications where the operating temperature range is important.

For further details on the power supply please refer to "i.CoreM6SX" data sheet and Reference Manual.

5.2.1 How to connect a backup battery

The module allows the use of lithium rechargeable battery or super-capacitor as backup battery.
The connection with module is obtained by connecting directly the backup battery to the +Vcoin signal (pin 18 floating if not used).

The consumption of the pin is given by NXP for a maximum of 275 uA

Note: *The module is already designed to manage the charge of backup battery.*

5.3 How to connect two 3-wire RS232 serial port

In this section is shown how to use the i.MX6SX UART1 and UART2 as 3-wire RS232 serial ports.
In the following table are shown the UART1 and UART2 pins numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
112	UART2_TXD	UART2 TXD signal	Y	+3,3V
113	UART2_RXD	UART2 RXD signal	Y	+3,3V
116	UART1_TXD *	UART1 TXD signal	Y	+3,3V
117	UART1_RXD *	UART1 RXD signal	Y	+3,3V

Table 9

The signals on the module's UART pins are 3.3V logic level, this can not be connected directly to a RS232 device like a PC Serial port, the use of a transceivers on the base board is mandatory in order to avoid module damage.

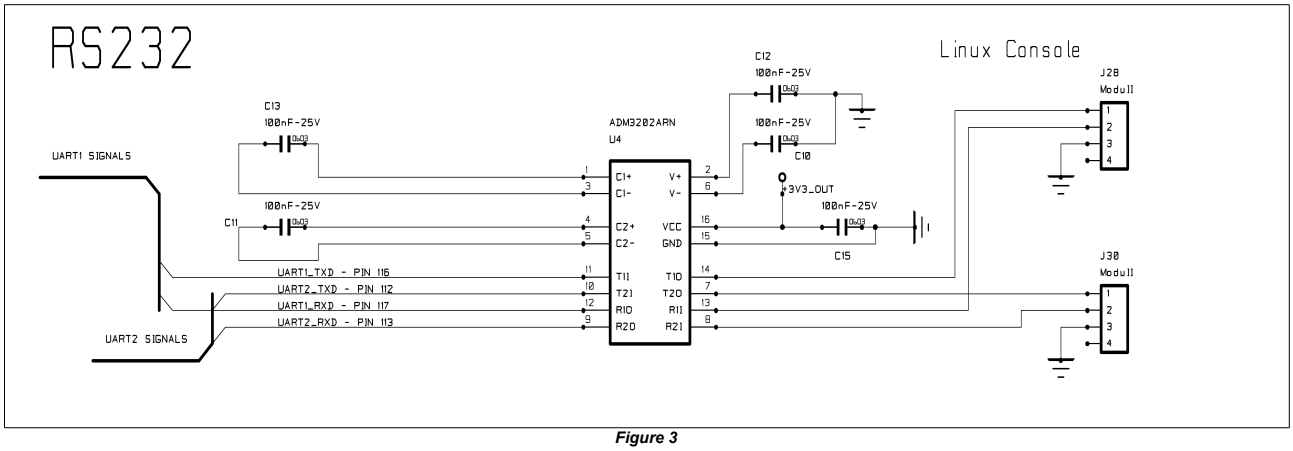


Figure 3

In the previous figure is shown how **UART1** and UART2 are connected in the i.MX6SX evaluation board. In this example an ADM3202ARN IC from Analog Device is used like transceiver for both UART without any control signal. In case RTS and CTS are need, a transceiver must be used for this signals.

When Linux is installed on a module, the UART (on module pin 116,117) is used like console. The default communications settings is shown in the table below.

Linux console default settings	
Baud rate	115200
Data length	8 bit
Parity	none
Stop	1bit

Table 10

* **Note**: *the UART1 is used as Linux Console*

5.4 How to connect a RS485 serial port

In this chapter is shown how an RS485 serial port can be connected to the module. In the figure below is shown how UART3 is used to connect to a RS485 transceiver on the starter kit. The figure shows UART3 connection but you can consider that also UART 4 & 5 can be used to connect a RS485 transceiver.

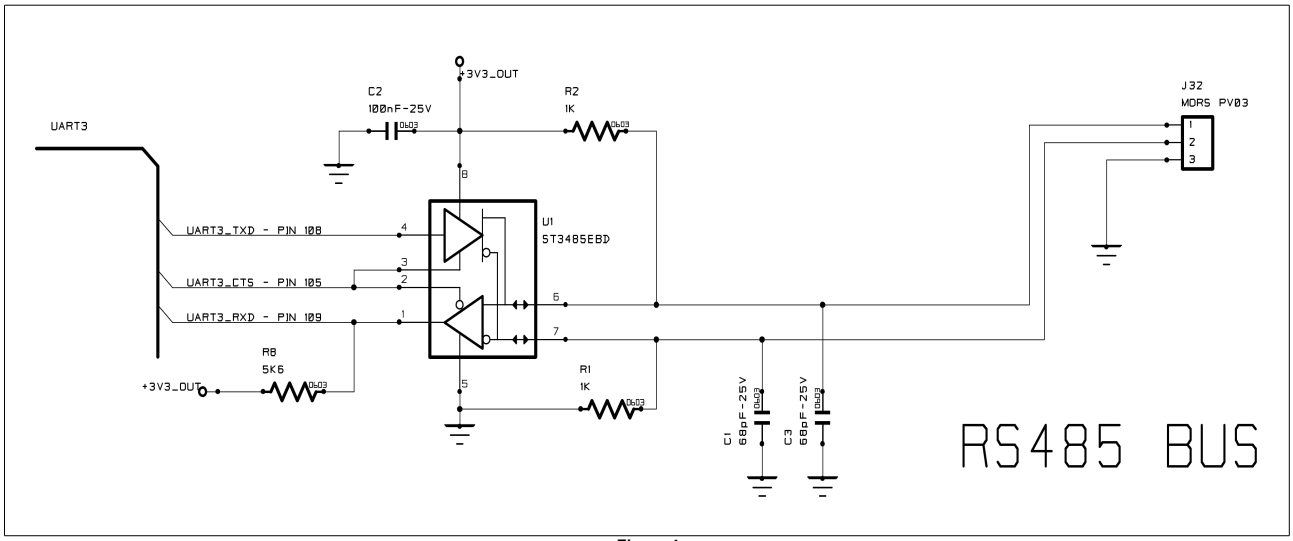


Figure 4

The pins involved in this RS485 communication example are listed in the following table.

Number	Name	Primary Function Description	GPIO Capable	Voltage
105	UART3_CTS	UART3 CTS signal	Y	+3,3V
106	UART3_RTS	UART3 RTS signal	Y	+3,3V
108	UART3_TXD	UART3 TXD signal	Y	+3,3V
109	UART3_RXD	UART3 RXD signal	Y	+3,3V

Table 11

5.5 How to connect CAN BUS interfaces

In this chapter is described how CAN bus transceiver can be connected to a i.MX6SX module. In the figure below is shown how CAN BUS 1 and 2 are connected in the evaluation board. Both CAN buses have been implemented.

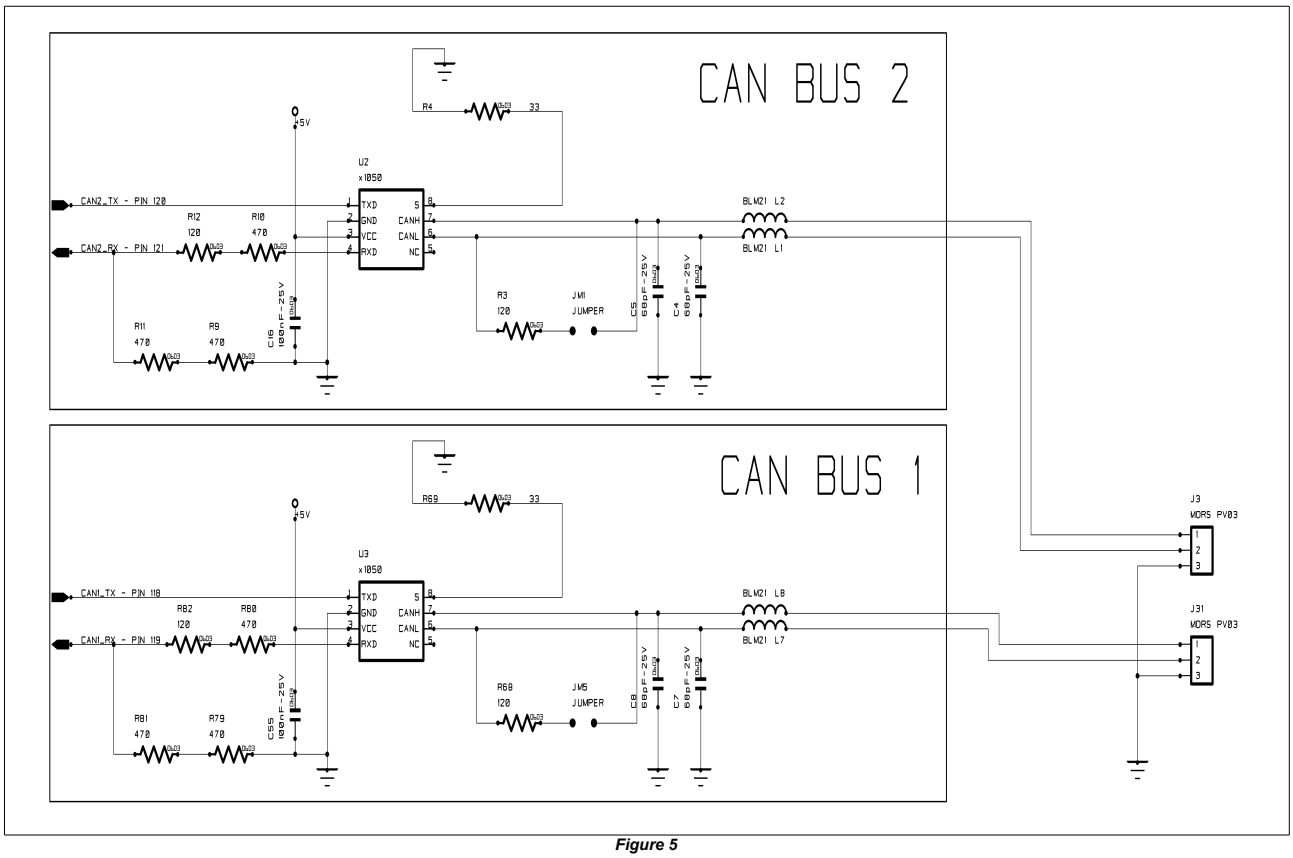


Figure 5

The following table describes the pins' numbering in the main connector involved in the CAN interface

Number	Name	Primary Function Description	GPIO Capable	Voltage
118	CAN1_TX	CAN 1 transmit signal	Y	+3,3V
119	CAN1_RX	CAN 1 receive signal	Y	+3,3V
120	CAN2_TX	CAN 2 transmit signal	Y	+3,3V
121	CAN2_RX	CAN 2 receive signal	Y	+3,3V

Table 12

The Jumpers JM1, JM5 are used to close the load of the CAN Bus to 120 Ω

5.6 How to design the Ethernet interface

The NXP i.MX6SX Ethernet Media Access Controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE standard 802.3™ networks. The 10-Mbps and 100-Mbps RMII Ethernet physical interfaces is supported. In the figure is shown how to connect the Ethernet interface to module.

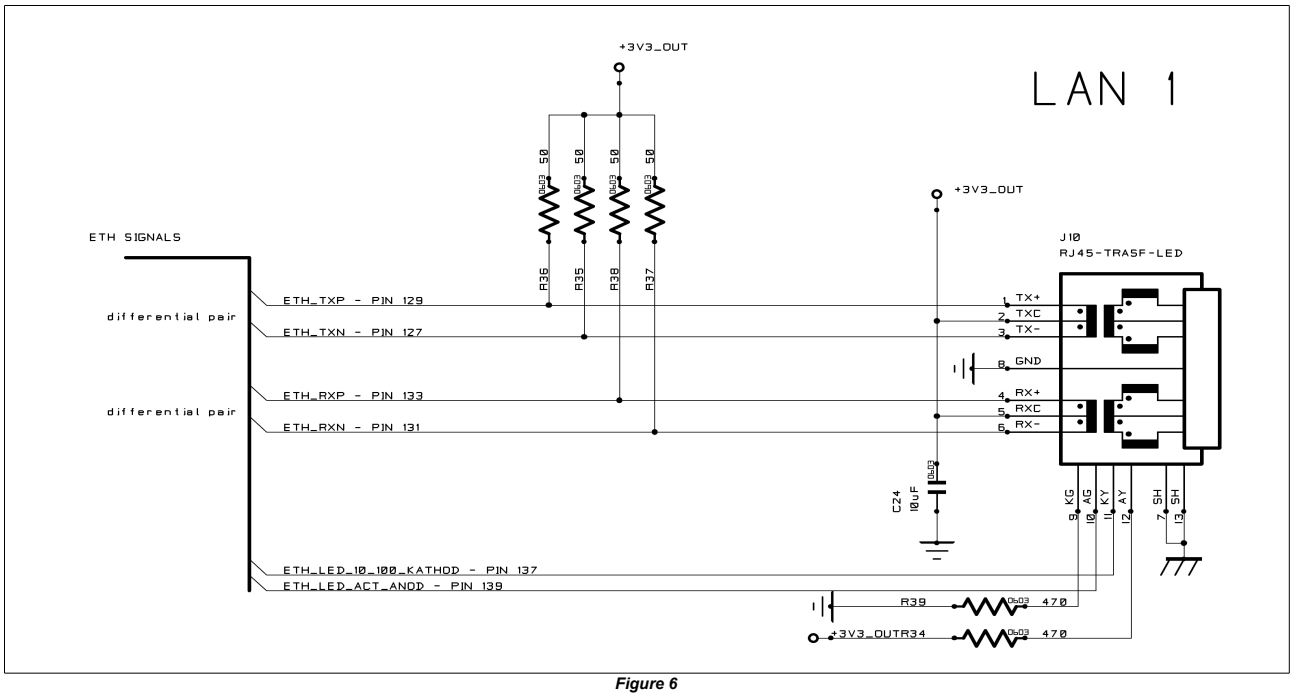


Figure 6

In the table below are listed all Ethernet signal of the module:

Number	Name	Primary Function Description	GPIO Capable	Voltage
127	ETH0_TXN	Fast Ethernet TXN signal	-	+3,3V
129	ETH0_TXP	Fast Ethernet TXP signal	-	+3,3V
131	ETH0_RXN	Fast Ethernet RXN signal	-	+3,3V
133	ETH0_RXP	Fast Ethernet RXP signal	-	+3,3V
137 *	ETH0_LED_10_100_KATHOD	Led Indicator Cathode	-	+3,3V
139 *	ETH0_LED_ACT_ANOD	Led indicator Anode signal	-	+3,3V
94	ETH1_TXP	Fast Ethernet TXP signal	-	+3,3V
96	ETH1_TXN	Fast Ethernet TXN signal	-	+3,3V
97	ETH1_LED_10_100_KATHOD	Led Indicator Cathode	-	+3,3V
98	ETH1_RXP	Fast Ethernet RXP signal	-	+3,3V
99 *	ETH1_LED_ACT_ANOD	Led indicator Anode signal	-	+3,3V
100 *	ETH1_RXN	Fast Ethernet RXN signal	-	+3,3V

Table 13

*** *Note:*** If not used, this pin must be left floating.

5.6.1 Component Placement considerations

Components placement can affect signal quality, emissions and can decrease EMI problems.

1. If the magnetics are a discrete component than the distance from the connector RJ45 should be kept to under 25mm of separation.
2. To decrease EMI problems the distance between magnetics and Phy should be at least 25mm or greater to isolate the PHY from magnetics.
3. The distance between Phy and RJ45 connector should always be within 200 mm.
4. The differential transmit pair should be keep at least 25mm from the edge of PCB up to the magnetics. If the magnetics are integrated into RJ45 the differential pair should be routed to the back of integrated magnetics RJ45 connector , away from the board of PCB.
5. The 49.9 ohm pull-up resistors on the differential lines should be placed within 10 mm of the Phy device
6. The signals RX & TX should be independently matched in length to within 6mm

See following figure

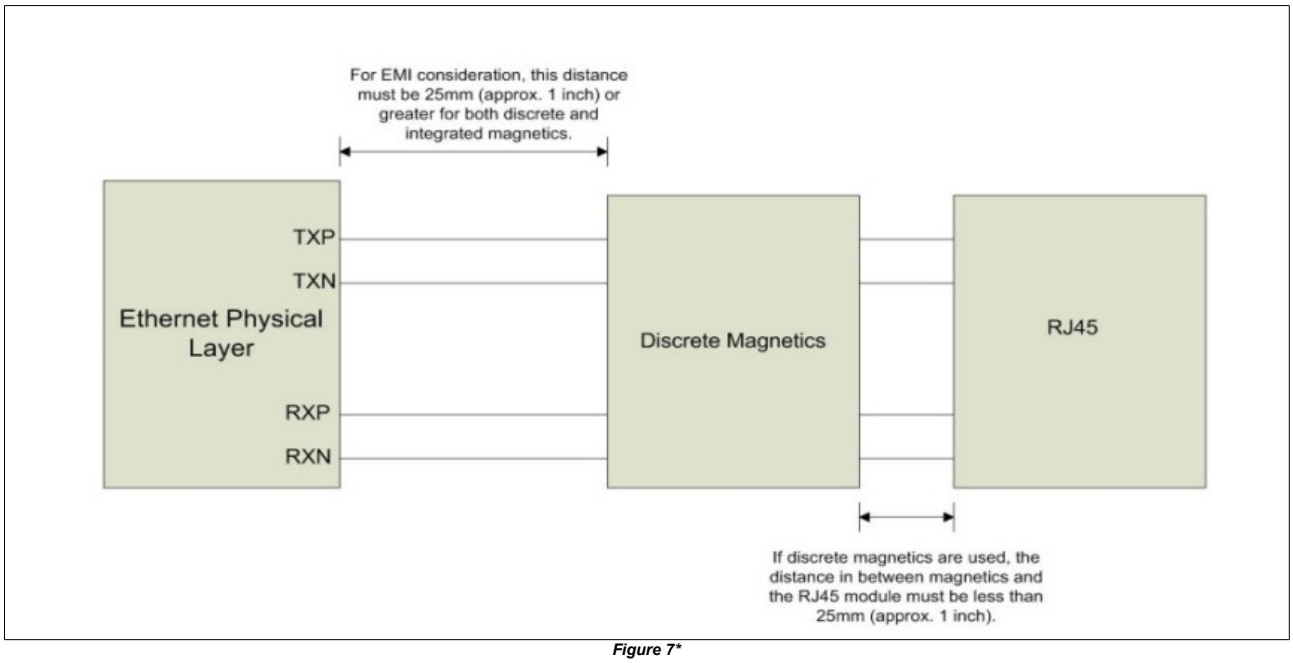


*Figure 7**

The PHY used in the module is the ***SMSC LAN8710***.
Please for more information refer to the ***SMSC Ethernet Physical Layer Layout Guidelines***.

For a list of magnetics selected to operate with the SMSC LAN8710, please refer to the Application note ***AN 8-13 Suggested Magnetics.***

*** this is the figure 2.3 from SMSC Ethernet Physical Layer Layout Guidelines**

5.6.2 Cable Transient Event and PHY Protection

Cable transient events are + and - DC surges that are induced across the transformer onto the PHY side of the TX+/- and RX+/- signals as shown in figure below. The PHY side of the transformer should not contain any DC component other than the typical 3.3V pull-up on the center tap of the transformer for analog signal biasing. In POE applications, there are two main reasons why cable transient events occur, negative rail PSE switching, and hot unplug/plug-in events.

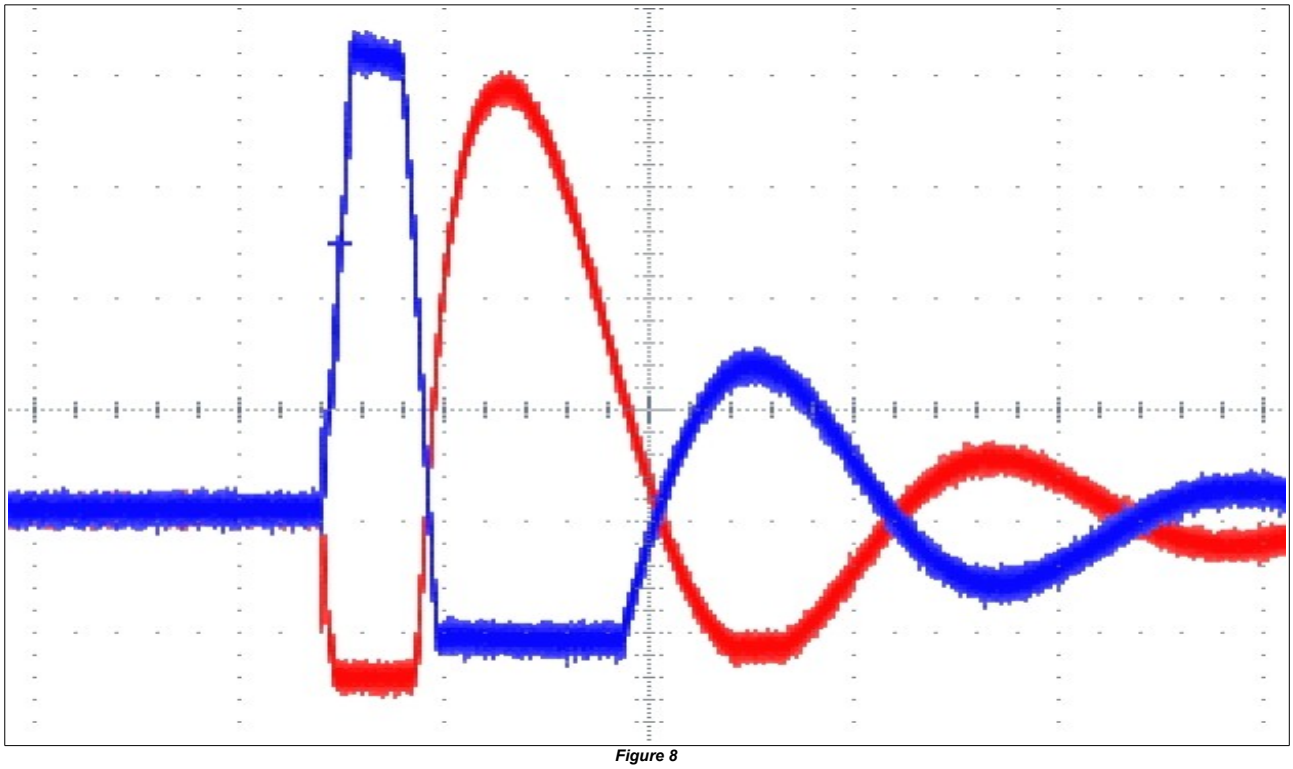


Figure 8

Transient observer on the PHY side of Eth Magnetics

Scale X = 1uS/div

Scale Y = 5V/div

Note: *for further details about Cable transient events please refers to file AN1718 of SMSC*

5.6.3 Phy Ethernet

When using an SMSC device in POE applications, external transient protection is recommended as shown in figure below. The schematic shows an example of a TVS suppression solution. This solution couples the energy differentially into the two TVS diodes on each differential pair. For cases when the transient is across the TX+/- pair in the figure below, the voltage is clamped at a value equivalent to the forward bias voltage across D1, plus the zener voltage of D2. This transient voltage must be clamped at a voltage no **greater than 5V**. D3 and D4 act the same way when the transient is across the RX+/- differential pair. The total capacitance seen by each differential pair must not exceed 50pF (25pF single ended).

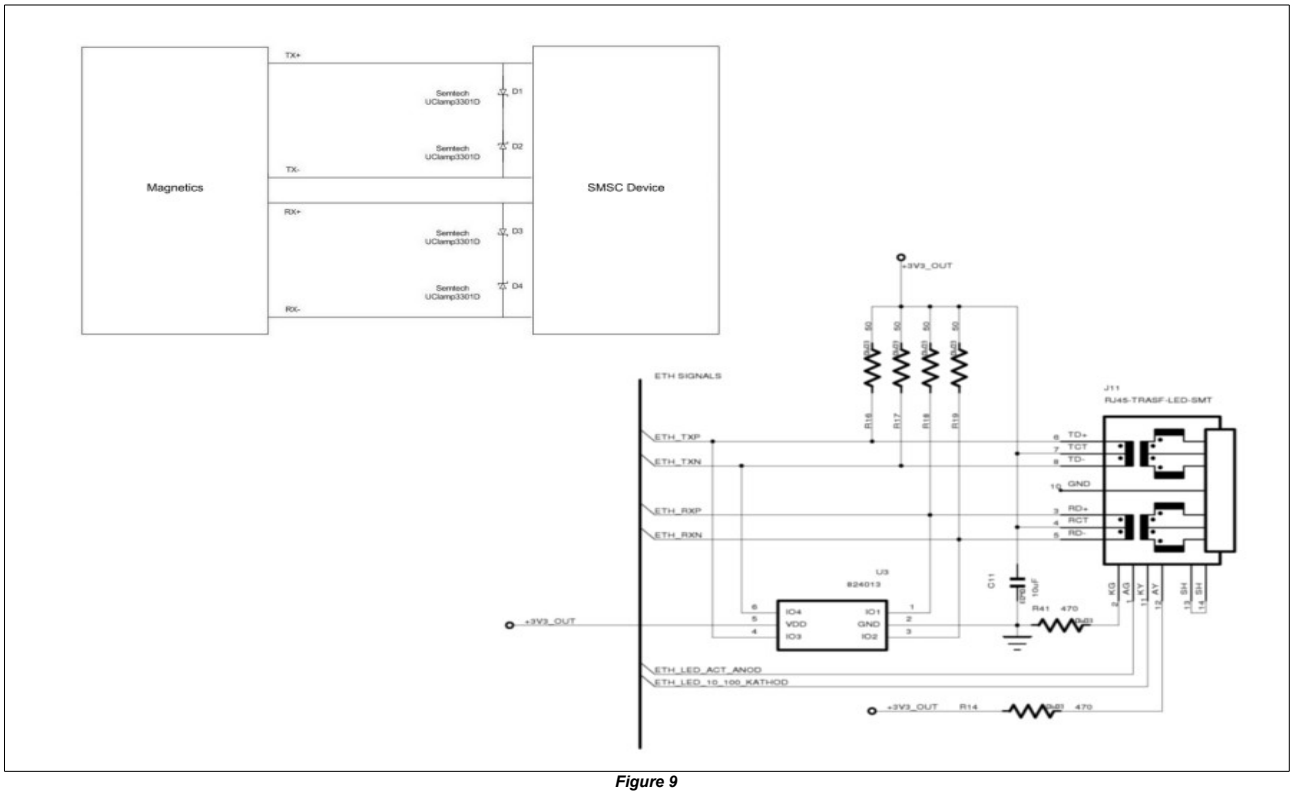


Figure 9

Recommended by ENGICAM:

Diode array TVS, 4 CH, ESD, 3.3V Wurth Elektronik 824013

Note: *for further details about PHY Protection please reffers to file AN1718 of SMSC*

5.7 USB interface

5.7.1 How to connect the USB OTG interface

The NXP i.MX6SX USB module provides high performance USB On-The-Go (up to 480Mbps), compatible with the USB 2.0 specification. An OTG HS PHY is also integrated so no external OTG PHY is needed on the baseboard. In the figure is shown how the MINI-AB USB/OTG connector is powered and connected in the evaluation board. In the following table are listed all USB/OTG signal of mail connector.

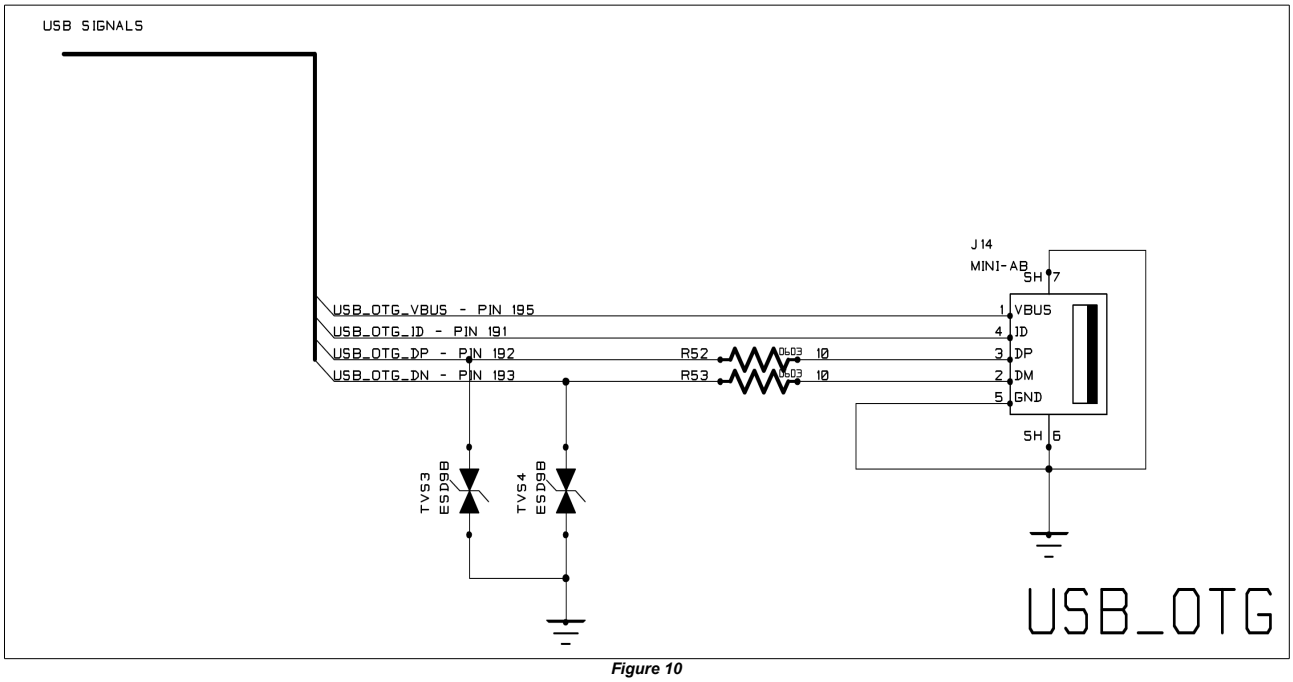


Figure 10

Number	Name	Primary Function Description	GPIO Capable	Voltage
195	USB_OTG_VBUS *	USB on the go interface	N	-
192	USB_OTG_DP	USB on the go interface	N	-
191	USB_OTG_ID	USB on the go interface	N	-
193	USB_OTG_DN	USB on the go interface	N	-

Table 14

**** Note: The USB_OTG_VBUS is an INPUT power signal. It must be connected to 5V***

In the following figures there are shown two different ways to connect the USB OTG interface that may be used to work as either a host or a device.

Use of the USB OTG port as a Host with its own dedicated supply. The ID signal is forced to GND

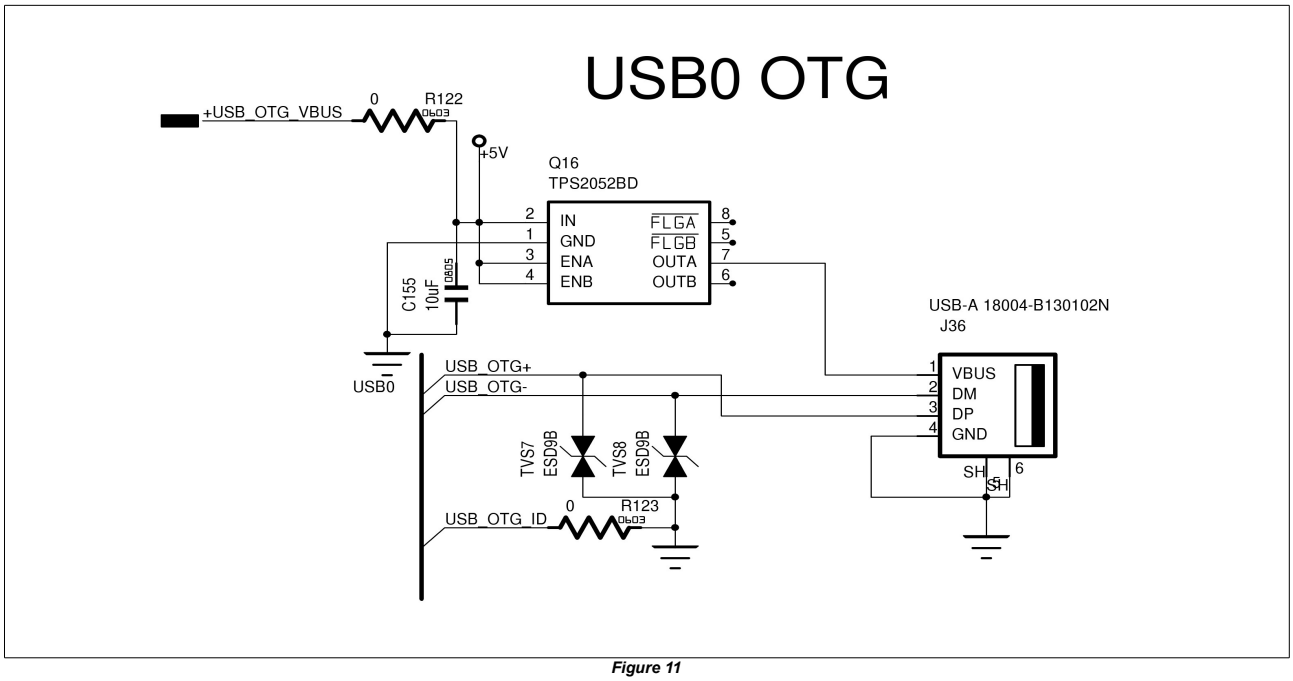


Figure 11

Use of the USB OTG port as Device or as Host depending on the status of the ID signal that is used also to enable the power supply.

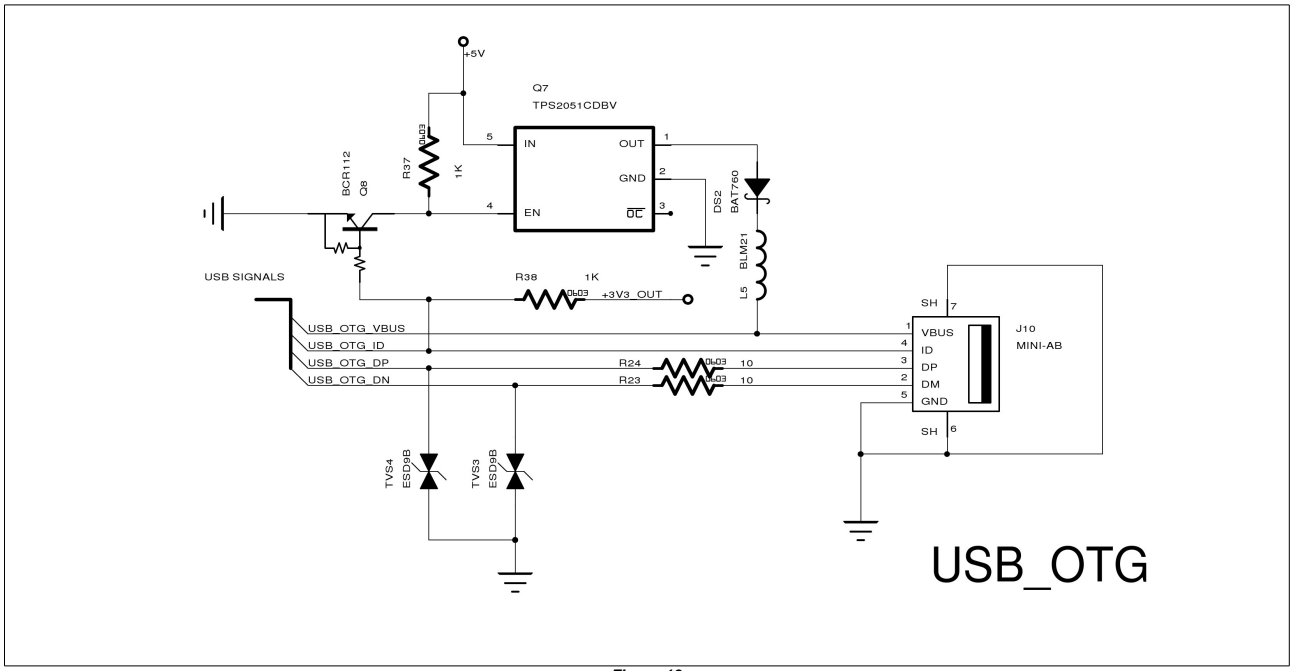


Figure 12

5.7.2 How to connect the USB host interface

The module provides one port for USB host interface. In the figure is shown how to connect this port to the Module.

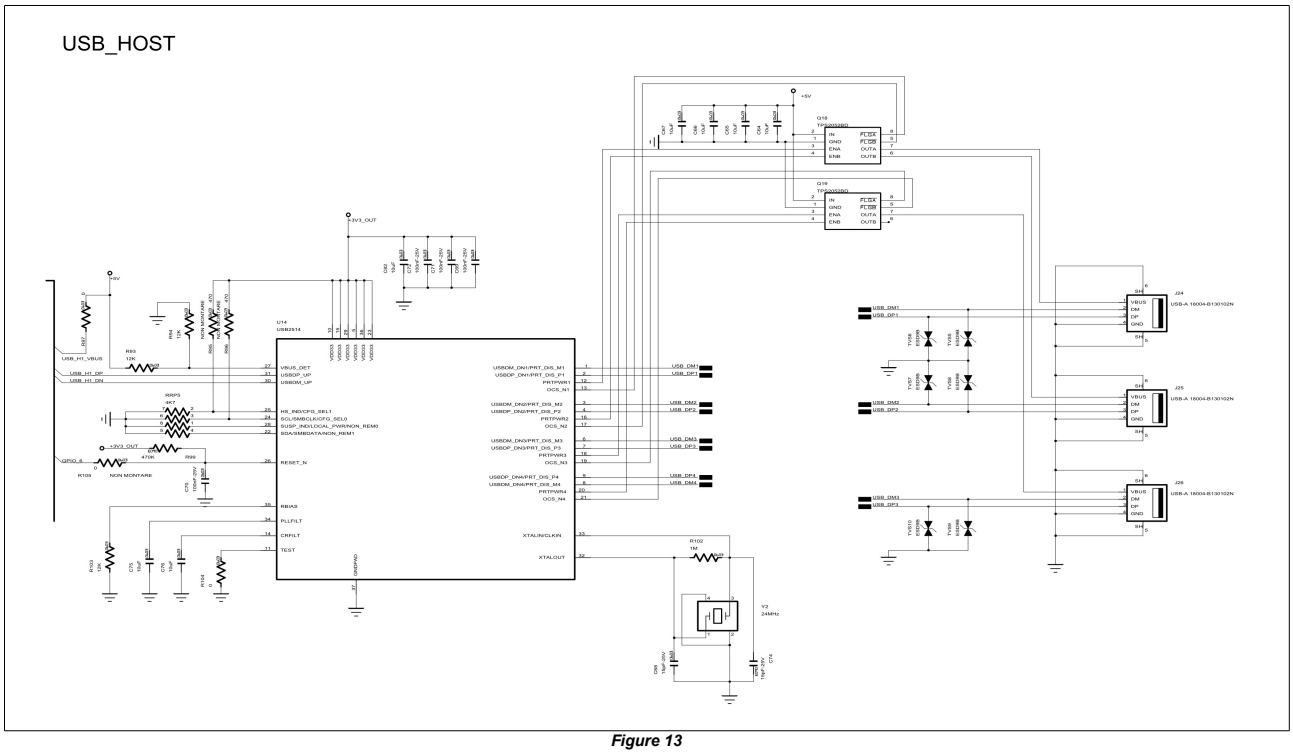


Figure 13

Engicam's evaluation board is equipped with an USB HUB to multiply the USB port available on module, if you just need one port you can connect it as one of the four output ports of the HUB

Number	Name	Primary Function Description	GPIO Capable	Voltage
180	USB_H1_VBUS *	USB HOST interface	N	-
194	USB_HI_DP	USB HOST interface	N	-
196	USB_H1_DN	USB HOST interface	N	-

Table 15

**** Note: The USB_H1_VBUS is an INPUT power signal. It must be connected to 5V***

5.8 How to connect the SD CARD interface

The NXP i.MX6SX's “enhanced Secured Digital Host Controller” (eSDHC) provides the interface between the host system and MMC/SD/SDIO/CE-ATA cards, including cards with reduced size or mini cards. The module include this features and in the figure is shown how the Micro SD Card connector is connected to i.MX6SX Module in the evaluation board. The eSDHC signal of the module's main connector are listed in table below.

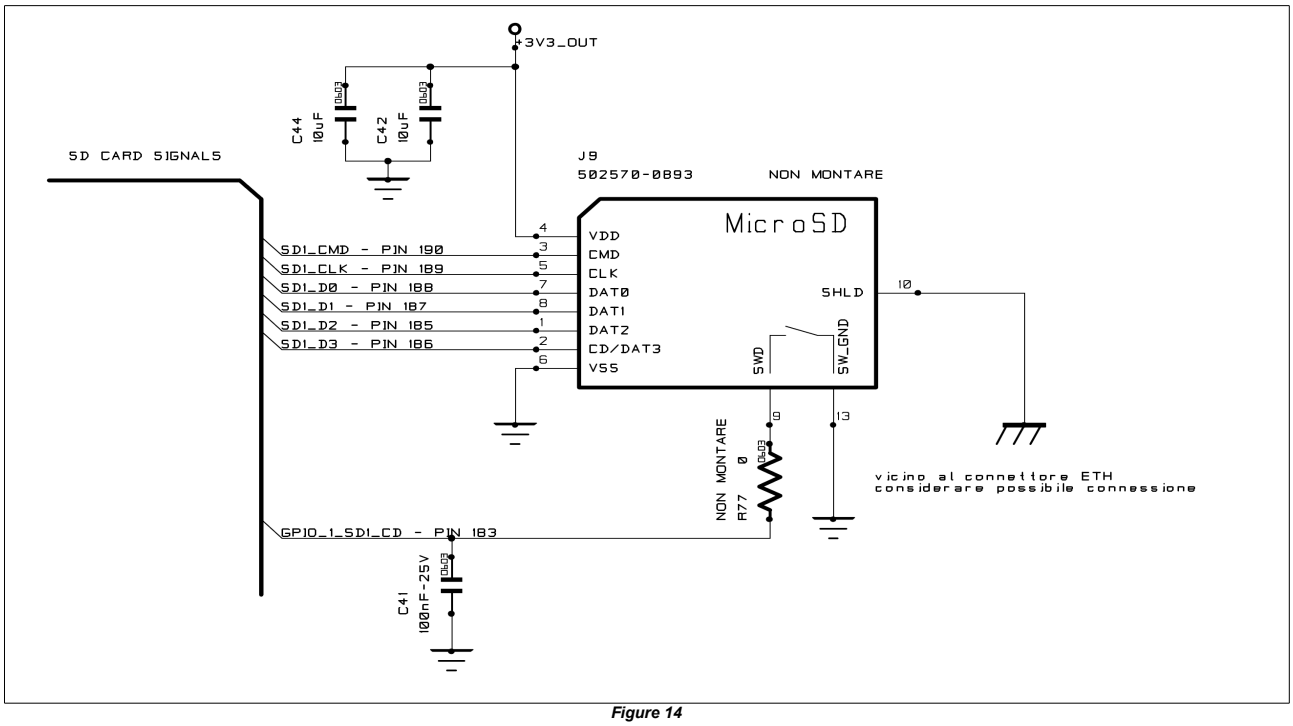


Figure 14

Number	Name	Primary Function Description	GPIO Capable	Voltage
183	SD1_CD	eSDHC CD Signal	Y	+3,3V
188	SD1_DAT0	eSDHC DAT 0 signal	Y	+3,3V
187	SD1_DAT1	eSDHC DAT 1 signal	Y	+3,3V
185	SD1_DAT2	eSDHC DAT 2 signal	Y	+3,3V
186	SD1_DAT3	eSDHC DAT 3 signal	Y	+3,3V
189	SD1_CLK	eSDHC CLK signal	Y	+3,3V
190	SD1_CMD	eSDHC CMD signal	Y	+3,3V
168	SD2_DAT0	eSDHC DAT 0 signal	Y	+3,3V
171	SD2_DAT1	eSDHC DAT 1 signal	Y	+3,3V
170	SD2_DAT2	eSDHC DAT 2 signal	Y	+3,3V
166	SD2_DAT3	eSDHC DAT 3 signal	Y	+3,3V
169	SD2_CLK	eSDHC CLK signal	Y	+3,3V
167	SD2_CMD	eSDHC CMD signal	Y	+3,3V

Table 16

5.9 How to connect an LCD display

The evaluation board of i.MX6SX is equipped with one RGB data port, this interface contains RGB data of 18 bit, pixel clock.
Following are reported the schematic interface with parallel URT and the map of signals.

Number	Name	Primary Function Description	GPIO Capable	Voltage
125	DISP0_CLK	LCD interface	Y	+3,3V
141	DISP0_D17	LCD interface	Y	+3,3V
142	DISP0_D16	LCD interface	Y	+3,3V
143	DISP0_D15	LCD interface	Y	+3,3V
144	DISP0_D14	LCD interface	Y	+3,3V
145	DISP0_D13	LCD interface	Y	+3,3V
146	DISP0_D12	LCD interface	Y	+3,3V
147	DISP0_D11	LCD interface	Y	+3,3V
148	DISP0_D10	LCD interface	Y	+3,3V
149	DISP0_D9	LCD interface	Y	+3,3V
150	DISP0_D8	LCD interface	Y	+3,3V
151	DISP0_D7	LCD interface	Y	+3,3V
152	DISP0_D6	LCD interface	Y	+3,3V
153	DISP0_D5	LCD interface	Y	+3,3V
154	DISP0_D4	LCD interface	Y	+3,3V
155	DISP0_D3	LCD interface	Y	+3,3V
157	DISP0_D2	LCD interface	Y	+3,3V
158	DISP0_D1	LCD interface	Y	+3,3V
159	DISP0_D0	LCD interface	Y	+3,3V
160	DISP0_VSYNC	LCD interface	Y	+3,3V
161	DISP0_HSYNC	LCD interface	Y	+3,3V
162	DISP0_DRDY	LCD interface	Y	+3,3V

Table 17

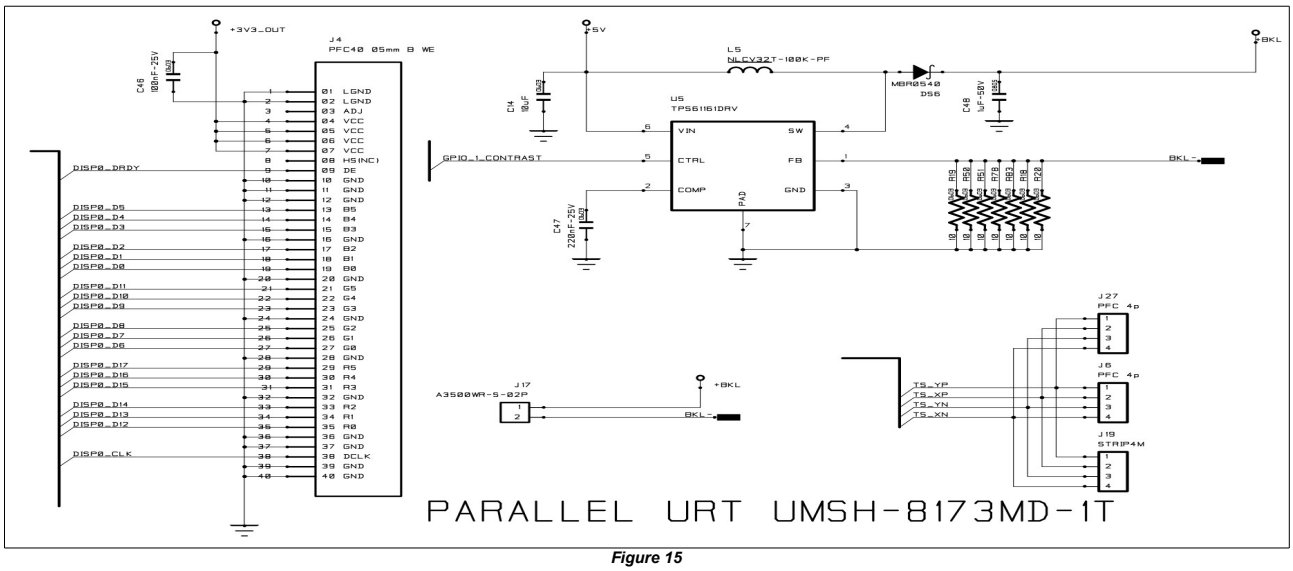


Figure 15

5.9.1 Connection map for 18 bit TFT only

The following map represent the connection mode applied to 18 bit TFT display. For every connection the colour controlled is joined

Number	Name	18 bit TFT connections	RGB
159	DISP0_D0	BLU 0	
158	DISP0_D1	BLU 1	
157	DISP0_D2	BLU 2	
155	DISP0_D3	BLU 3	
154	DISP0_D4	BLU 4	
153	DISP0_D5	BLU 5	
152	DISP0_D6	GREEN 0	
151	DISP0_D7	GREEN 1	
150	DISP0_D8	GREEN 2	
149	DISP0_D9	GREEN 3	
148	DISP0_D10	GREEN 4	
147	DISP0_D11	GREEN 5	
146	DISP0_D12	RED 0	
145	DISP0_D13	RED 1	
144	DISP0_D14	RED 2	
143	DISP0_D15	RED 3	
142	DISP0_D16	RED 4	
141	DISP0_D17	RED 5	

Table 18

5.9.2 LVDS Interfaces

In the module there is only one connection to display with LVDS interface, the connection is up to 24 bit data. The Evaluation board is design to 18 bit LVDS interface only.
Following the LVDS interfaces maps and schemes

Number	Name	Primary Function Description	GPIO Capable	Voltage
42	LVDS_TX3_P	LVDS Interface's Signals	N	+2V5
44	LVDS_TX3_N	LVDS Interface's Signals	N	+2V5
46	LVDS_CLK_P	LVDS Interface's Signals	N	+2V5
48	LVDS_CLK_N	LVDS Interface's Signals	N	+2V5
50	LVDS_TX1_P	LVDS Interface's Signals	N	+2V5
52	LVDS_TX1_N	LVDS Interface's Signals	N	+2V5
58	LVDS_TX2_P	LVDS Interface's Signals	N	+2V5
59	LVDS_TX0_P	LVDS Interface's Signals	N	+2V5
60	LVDS_TX2_N	LVDS Interface's Signals	N	+2V5
61	LVDS_TX0_N	LVDS Interface's Signals	N	+2V5

Table 19

In the figure below is shown LVDS port. The not mount resistors is needed to drive TFT with only 3 LVDS “channel” this means drive TFT at 18 bit instead of 24 bit. The channel is referred to the pair signal “P” & “N”.

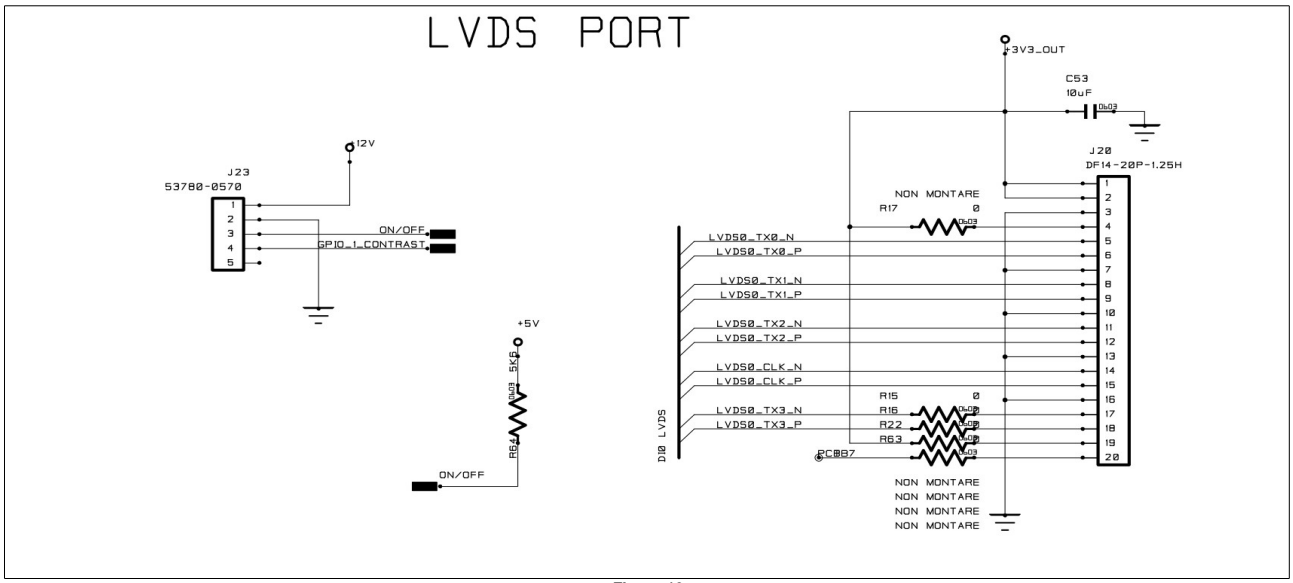


Figure 16

5.9.3 LVDS Routing and Placement Considerations

The LVDS lines are high-speed signals and as such during the designing must be complied with standards of protection against noise and crosstalk. In this chapter we give some advices about positioning, cabling and routing; for further details please follow the guidelines and the manuals about LVDS bus.
Differential line: as mentioned we are working with fast signals, then to avoid disturbances and reduce noise on the line we suggest to route the channel lines in differential mode, for the same reason also the “channel” on the cable used to connect the board to TFT should be twisted.
Distance: there is no distance recommended between the devices but, always considering the nature of signals and that the driver is the same processor i.MX6SX, we suggest to positioning the connector as close as possible to the module, and also to be aware to matching the line of differential pair as best as you can to avoid any kind of delay.
Controlled Impedance: all the signal's pairs must be traced in controlled impedance referred to the GND plane. This should avoid the problems due to reflections on the line. We suggest that the traces for LVDS signals should be closely-coupled and designed for 100Ω differential impedance.

Note: for further informations consult differential micro-strips and high speed routing documentations

5.10 How to connect the PCIe interface

PCIe 2.0 PHY is a complete mixed-signal semiconductor intellectual property solution, designed for single-chip integration into computer applications. The PCIe2 PHY ssp_x1 includes all the necessary logical, geometric and physical design files to implement complete PCI Express 2.0 physical layer capability for 5Gb/s operation, connecting a host controller or device controller to a PCI Express system. This product is optimized for a system-on-Chip (SoC) design targeted to the TSMC 40LP1.1/2.5-V fabrication process.

The PCIe 2.0 PHY supports both the 5 Gbp/s data rate of the PCI Express Gen 2.0 specifications as well as being backwards compatible to the 2.5Gb/s Gen 1.1 specification.

Number	Name	Primary Function Description	GPIO Capable	Voltage
67	PCIe_RXM	PCIe_RXM	N	-
69	PCIe_RXP	PCIe_RXP	N	-
72	PCIe_TXM	PCIe_TXM	N	-
74	PCIe_TXP	PCIe_TXP	N	-
76	PCIe_REFCLKM	PCIe_REFCLKM	N	-
78	PCIe_REFCLKP	PCIe_REFCLKP	N	-

Table 20

It's strongly recommended to positioning the capacitor of PCIe signals as close as possible to the connector. Capacitors on RX signals may be unnecessary and replaceable with 0 Ohm resistors

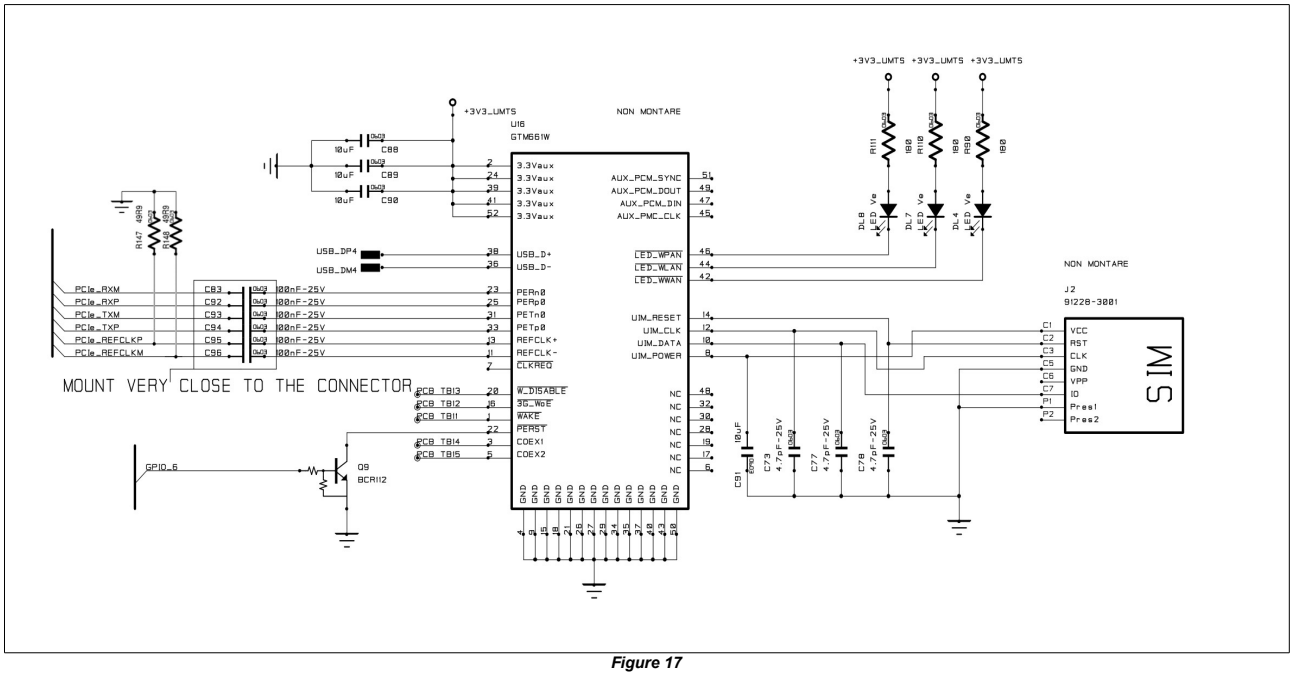


Figure 17

Termination is required on the differential clock lines. Connect two 49.9 Ω resistors, one between REFCLK and GND, the other between REFCLK+ and GND. Alternately, Connect a 100 Ω resistor between REFCLK- and REFCLK+, as close as possible to the receiver device (connector).

Note: *for further details please refer to PCIe recommendations on* ***iMx6*** *series document (as design guide IMX6SXHDG and reference manual).*

5.11 JTAG Interface

Joint Test Action Group (**JTAG**) is the common name used for the IEEE 1149.1 standard entitled **Standard Test Access Port and Boundary-Scan Architecture** for test access ports used for testing printed circuit boards using boundary scan. JTAG is often used as an IC debug or probing port.

There are no official standards for JTAG adapter physical connectors. Development boards usually include a header to support preferred development tools; in some cases they include multiple such headers, because they need to support multiple such tools. For example, a micro-controller, FPGA, and ARM application processor will rarely share tools, so a development board using all of those components might have three or more headers. Production boards may omit the headers; or when space is tight, just provide JTAG signal access using test points.

In the figure below is shown how to connect a JTAG interface to i.MX6SX Module.

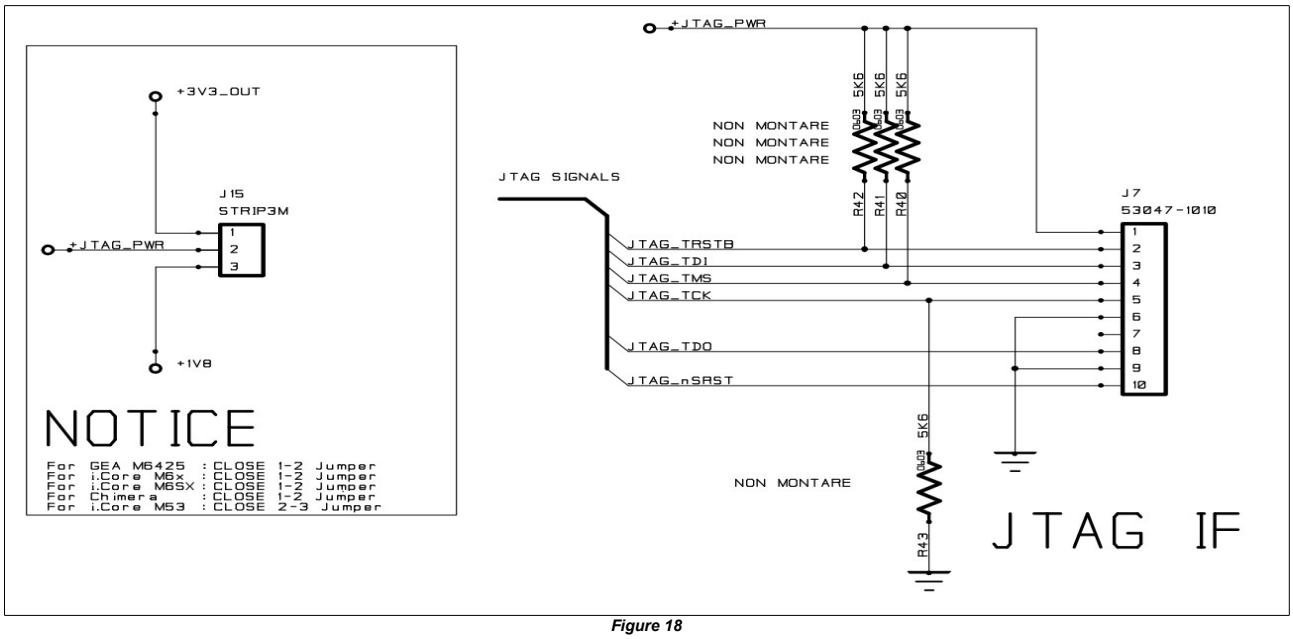


Figure 18

In the table are listed all JTAG signals as mapped in the main connector.

Number	Name	Primary Function Description	GPIO Capable	Voltage
173	JTAG_TRSTB	JTAG Interface	N	+3,3V
174	JTAG_TDO	JTAG Interface	N	+3,3V
175	JTAG_TDI	JTAG Interface	N	+3,3V
176	JTAG_TMS	JTAG Interface	N	+3,3V
177	JTAG_TCK	JTAG Interface	N	+3,3V
179	JTAG_nSRST	JTAG Interface with Pull-up on module	N	+3,3V

Table 21

To obtain the compatibility with i.MX53 Module, in the evaluation board of the i.MX6SX the JTAG signals are pulled up through +JTAG_PWR which could be put to +1,8V or +3,3V using jumper referenced J15.
If you intend to use both module on your main board and don't use a JTag external console is mandatory to remove the pull-up/down resistors.

Please for further details refer to i.MX6SX reference manual.

5.12 Boot Mode Pin

Boot mode pin determines how the module boot. The following table listed the possible options of the boot mode:

BOOT_MODE	Action
0	Boot from internal modules
1	Boot from USB OTG

Table 22

The boot from USB OTG is usually used for the boot loader deploy.

In the figure is shown the Evaluation board's boot section also compatible with iCoreM53 module. The closing of JM2 corresponds to put at logical 1 the boot mode pin. Also in this case to switch from iCoreM53 module to i.MX6SX module is necessary to use the J15 jumper to set the right value of the voltage.

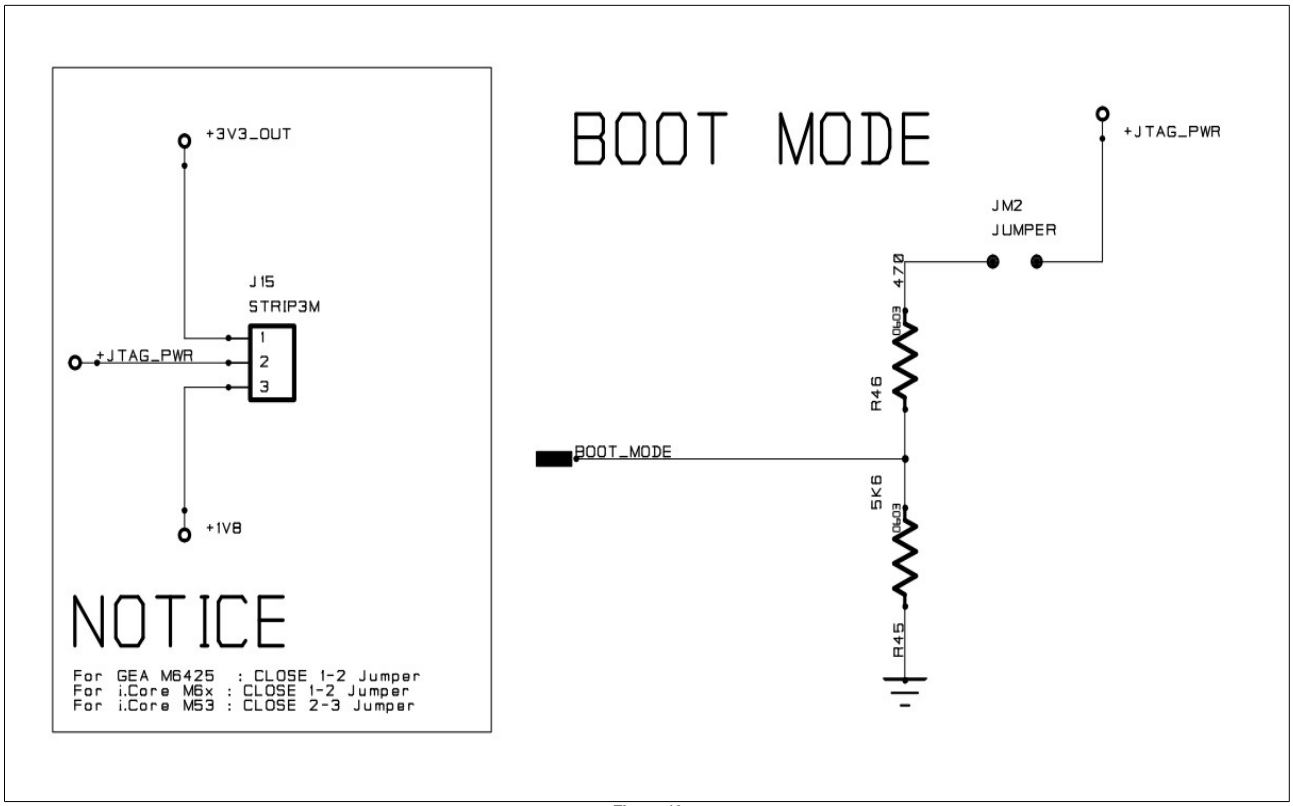


Figure 19

Number	Name	Primary Function Description	GPIO Capable	Voltage
181	BOOT_MODE	Boot from USB/UART or on board Nand Flash	N	-

Table 23

In the evaluation board we set-up all the configurations for bootstrap from NAND and from SD card.

In the figure below is shown the boot options configurations for i.MX6SX on the Evaluation board.

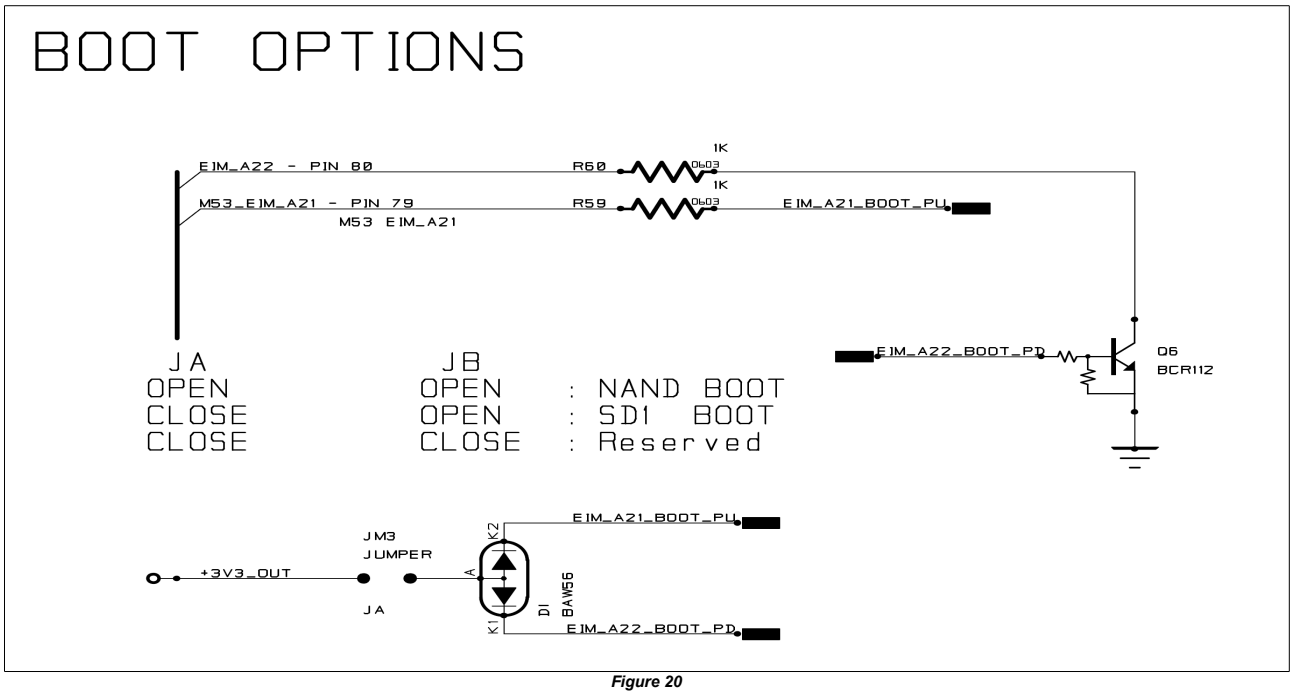


Figure 20

The figure above shows the implementation of the boot option applied to the EVABOARD. The signal used to configure the boot is on pin 80. The signal nSD_BOOT on pin 80 is pulled up on the module with 12KOhm resistor.
In the standard condition this signal in the evaluation board is setting to boot from NAND Flash (jumper left open), or from SD card simply closing the jumper.
Following you can see the signals logical level to implement a custom starting sequence. The first sequence is already implemented in the module.

BOOT FROM NAND	
Signal	**LOGIC LEVEL**
nSD_BOOT	1

Table 24

The choice of boot from SD means short-cutting the jumper A in the evaluation board.

BOOT FROM SD1	
Signal	**LOGIC LEVEL**
nSD_BOOT	0

Table 25

In the evaluation board whatever starting sequence you chose you must consider the pins 80 of main connector useful for boot configuration.

Note: for using of any customized boot options please refer to the NXP reference manual of i.MX6SoloX

5.12.1 Boot Signals Management

Following are shown the signals you must consider during the boot sequence:

Signal	SODIMM Pin number	Status on Reset (*Mandatory*)	Boot Config Signal	Boot eFUSE Descriptions
DISP0_D0	159	PU or Floating	BOOT_CFG1[0]	
DISP0_D1	158	PD or Floating	BOOT_CFG1[1]	
DISP0_D2	157	PD or Floating	BOOT_CFG1[2]	
DISP0_D3	155	PD or Floating	BOOT_CFG1[3]	
DISP0_D4	154	Floating	BOOT_CFG1[4]	
DISP0_D5	153	Floating	BOOT_CFG1[5]	
DISP0_D6	152	Floating	BOOT_CFG1[6]	
DISP0_D7	151	Floating	BOOT_CFG1[7]	
DISP0_D8	150	PD or Floating	BOOT_CFG2[0]	
DISP0_D9	149	PD or Floating	BOOT_CFG2[1]	
DISP0_D10	148	PD or Floating	BOOT_CFG2[2]	
DISP0_D11	147	PD or Floating	BOOT_CFG2[3]	
DISP0_D12	146	PD or Floating	BOOT_CFG2[4]	
DISP0_D13	145	PU or Floating	BOOT_CFG2[5]	
DISP0_D14	144	PD or Floating	BOOT_CFG2[6]	
DISP0_D15	143	PD or Floating	BOOT_CFG2[7]	
DISP0_D16	142	Floating	BOOT_CFG4[0]	
DISP0_D17	141	Floating	BOOT_CFG4[1]	
DISP0_CONTRAST	132	Floating	BOOT_CFG4[7]	

Table 26

Basing on the test result Engicam currently suggest to leave all these signals floating during reset status and **it's strongly recommended to consult the NXP's documentation before starting the carrier board design.**

WARNING:

please always refer to the NXP's documentations to design and configure the listed BOOT_CFG signals of your own board

5.13 Touch Screen Controller

Touch screen signals are implemented on MAX11801 Touch-Screen Controllers. The devices contain a 12-bit SAR ADC and a multiplexer to interface with a resistive touch-screen panel. The MAX11801's reference voltage for Touch screen signals is +3,3V

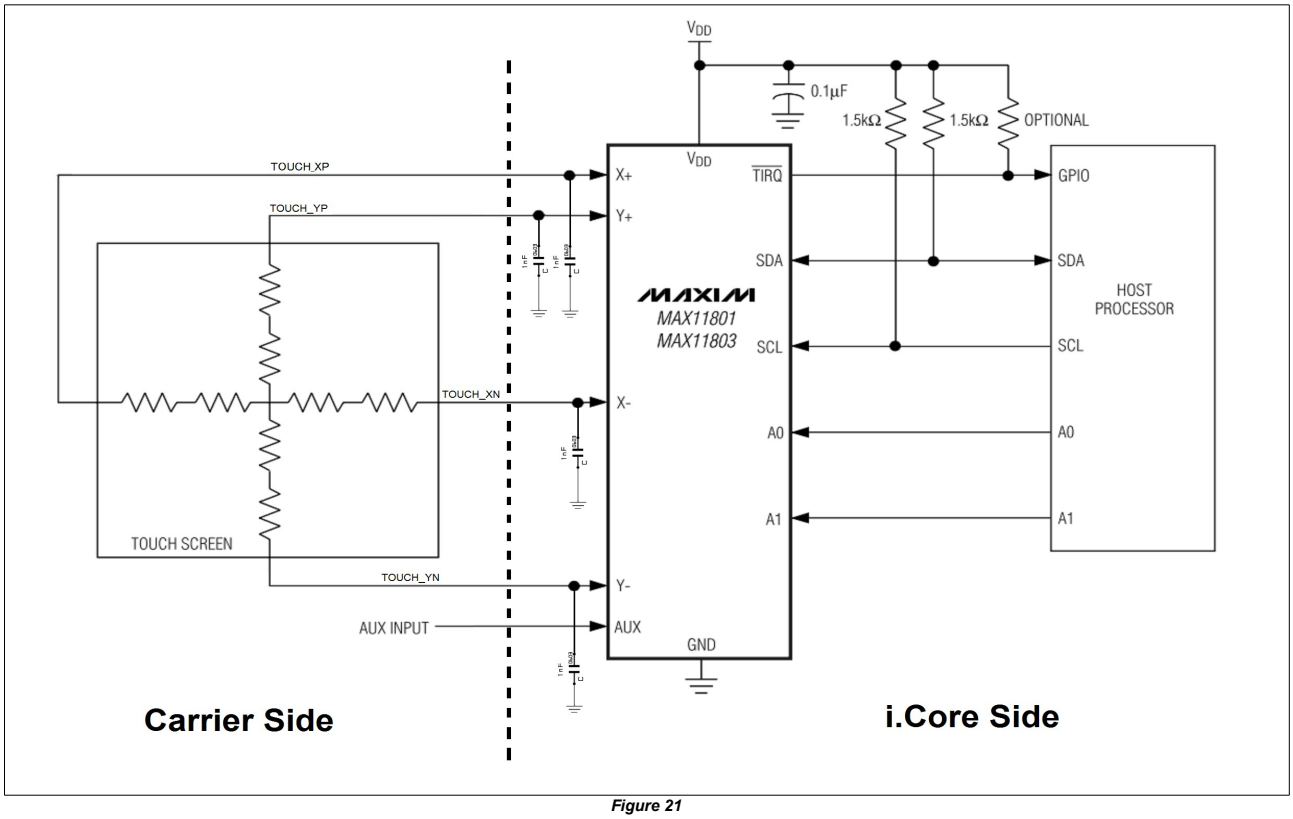


Figure 21

Number	Name	Primary Function Description	GPIO Capable	Voltage
25	TOUCH_XP	Touch Screen Xp	-	+3,3V
26	TOUCH_XN	Touch Screen Xn	-	+3,3V
27	TOUCH_YP	Touch Screen Yp	-	+3,3V
28	TOUCH_YN	Touch Screen Yn	-	+3,3V

Table 27

WARNING:
Is strongly recommended to put in the carrier board's layout a ceramic capacitor per signal line (X, Y P/N) as close as possible to SODIMM connector. Through the adjust of capacitor value it's possible to improve the disturbance due to noise on X/Y signals.

Note: a 1nF capacitor is already present on each line of the i.CoreM6SoloX modules but it could not be enough to suppress noise.

5.14 How to connect the reset pin

The nRESET signal has input/output functionality and shall be driven in open-drain mode. *The signal has an internal 100K pull-up and a 100 Ohm series resistors,the maximum recommended capacitive load is about **100pF**.*

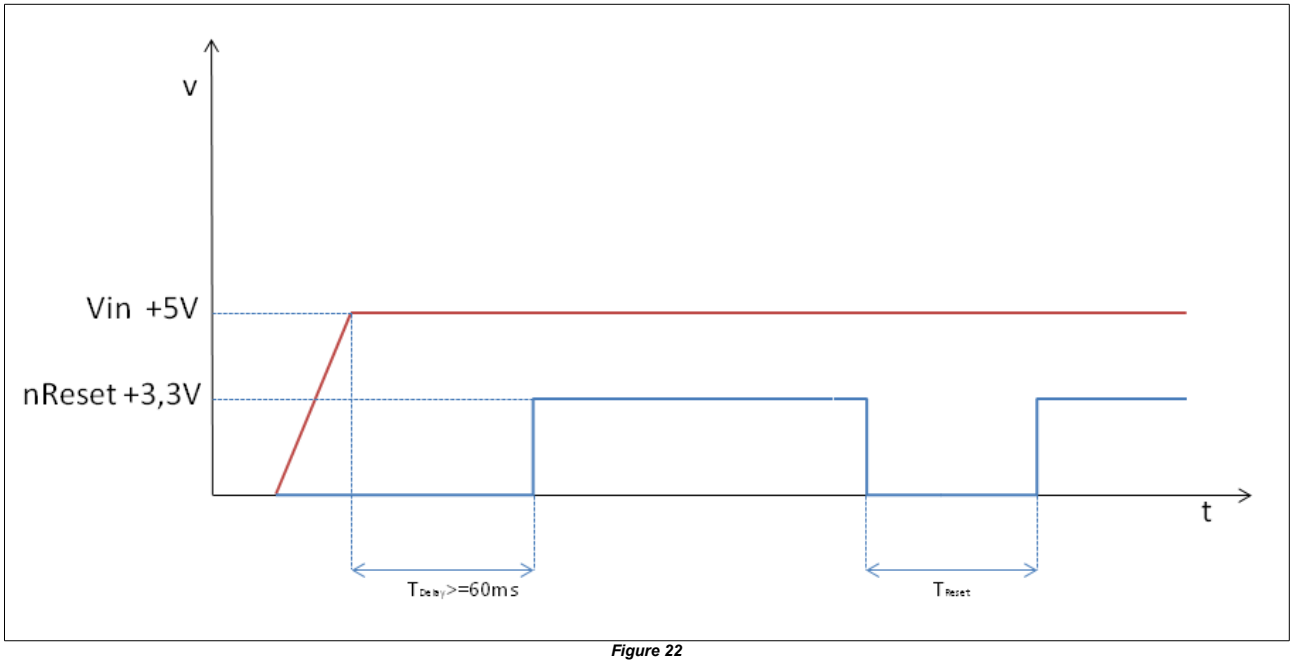


Figure 22

T_{Delay}: driven low by SOM during the POR state
T_{Reset}: driven low by user to force POR CPU pin

5.14.1 Input mode usage

The nRESET signal can be used to reset the module by driving it with an **open-drain** or with a simple button. If there are no special requirements, the module is fully auto-sufficient in terms of reset sequence, so its nRESET signal can be left floating. No Pull-up resistor is required on the carrier board; if a different pull-up resistor value (from the 100K on board of the module) is necessary, an additional pull-up on the carrier can be placed with values greater than 10K Ohm.

5.14.2 Output mode usage

The nRESET signal can also be used to monitor POR phase of the module, or to apply the reset (POR only) to other devices on the carrier. In this case, please take care to always respect limits imposed by maximum capacitive load and minimum additional pull-up.

WARNING: nReset is a POR signal only, therefore it may not be driven by the SOM during another CPU reset event (e.g. WDOG reset).

Chapter

6

6. Peripheral multiplexing

This Chapter gives the alternative peripheral informations

Section includes :

- ✔ **I2S**
- ✔ **SPI - QSPI**
- ✔ **PWM**
- ✔ **GPT and I2C**
- ✔ **UART**

6.1 Peripheral multiplexing description

Following we describe opportunity to use alternative interfaces using the properties of multiplexing pin.
Please refer to the NXP's reference manual and documentation for further details (document name i.MX6SoloXRM).

6.1.1 SPI & IIS Configuration

Using pin multiplexing 's features we may have the following SPI and IIS connections. In the tables below are shown the output signals on the Connector's module.

ECSPI1 signals interfaces +3,3V

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
66 / 86	KEY_ROW0 / QSPI1A_DATA0	MOSI	+3,3V
62 / 88	KEY_COL1 / QSPI1A_DATA1	MISO	+3,3V
82 / 130	QSPI1A_SCLK / KEY_COL0	SCK	+3,3V
63 / 68	QSPI1A_SS0_B / KEY_ROW1	SS0	+3,3V
35	KEY_ROW3	SS1	+3,3V
95	KEY_COL3	SS2	+3,3V
79	KEY_ROW2	SS3	+3,3V

Table 28

ECSPI3 signals interfaces +3,3V

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
105	QSPI1B_DATA0	MOSI	+3,3V
106	QSPI1B_DATA1	MISO	+3,3V
109	QSPI1B_SCLK	SCK	+3,3V
108	QSPI1B_SS0_B	SS0	+3,3V

Table 29

ECSPI4 signals interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
51 / 167	SD3_CMD / SD2_CMD	MOSI	+3,3V
122 / 166	SD3_DATA3 / SD2_DATA3	MISO	+3,3V
37 / 169	SD3_CLK / SD2_CLK	SCK	+3,3V
115 / 170	SD3_DATA2 / SD2_DATA2	SS0	+3,3V
186	SD1_DATA3	SS1	+3,3V
171	SD2_DATA1	SS2	+3,3V
168	SD2_DATA0	SS3	+3,3V

Table 29

ECSPI5 signals interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
84	QSPI1A_DQS	MOSI	+3,3V
65	QSPI1A_SS1_B	MISO	+3,3V
53	QSPI1B_SS1_B	SCK	+3,3V
54	QSPI1B_DQS	SS0	+3,3V
90	QSPI1A_DATA2	SS1	+3,3V
92	QSPI1A_DATA3	SS2	+3,3V
56	QSPI1B_DATA3	SS3	+3,3V

Table 30

QSPI1A

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
63	QSPI1A_SS0_B	QSPI1A_SS0	+3,3V
65	QSPI1A_SS1_B	QSPI1A_SS1	+3,3V
82	QSPI1A_SCLK	QSPI1A_SCLK	+3,3V
84	QSPI1A_DQS	QSPI1A_DSQ	+3,3V
86	QSPI1A_DATA0	QSPI1A_DATA0	+3,3V
88	QSPI1A_DATA1	QSPI1A_DATA1	+3,3V
90	QSPI1A_DATA2	QSPI1A_DATA2	+3,3V
92	QSPI1A_DATA3	QSPI1A_DATA3	+3,3V

Table 31

QSPI1B

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
108	QSPI1B_SS0_B	QSPI1B_SS0	+3,3V
53	QSPI1B_SS1_B	QSPI1B_SS1	+3,3V
109	QSPI1B_SCLK	QSPI1B_SCLK	+3,3V
54	QSPI1B_DQS	QSPI1B_DSQ	+3,3V
105	QSPI1B_DATA0	QSPI1B_DATA0	+3,3V
106	QSPI1B_DATA1	QSPI1B_DATA1	+3,3V
55	QSPI1B_DATA2	QSPI1B_DATA2	+3,3V
56	QSPI1B_DATA3	QSPI1B_DATA3	+3,3V

Table 32

The following tables show the pin configurations for IIS Bus on module's connector.

IIS bus interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
114 / 168	SD3_DATA0 / SD2_DATA0	I2S_DIN	+3,3V
122 / 166	SD3_DATA3 / SD2_DATA3	I2S_DOUT	+3,3V
124 / 171	SD3_DATA1 / SD2_DATA1	I2S_SCLK	+3,3V
34	SD4_RESET_B	I2S_MCLK	+3,3V
115 / 170	SD3_DATA2 / SD2_DATA2	I2S_LRCLK	+3,3V

Table 33

6.1.2 Alternative PWM pins table

It's possible to set the pins shown in the following table as PWM signals.

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
168 / 191	SD2_DATA0 / GPIO1_IO10	PWM1_OUT	+3,3V
171 / 184	SD2_DATA1 / GPIO1_IO11	PWM2_OUT	+3,3V
36 / 185	GPIO1_IO12 / SD1_DATA1	PWM3_OUT	+3,3V
38 / 187	GPIO1_IO13 / SD1_DATA1	PWM4_OUT	+3,3V
10	CSI_DATA04	PWM5_OUT	+3,3V
11	CSI_DATA05	PWM6_OUT	+3,3V

Table 34

6.1.3 General Purpose Timer (GPT)

Using pin multiplexing 's features we may have the following GPT and IIC connections. In the tables below are shown the output signals on the Connector's module.

GPT IN interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
188	SD1_DATA0	GPT_CAPTURE1	+3,3V
187	SD1_DATA1	GPT_CAPTURE2	+3,3V
189	SD1_CLK	GPT_CLK	+3,3V
190	SD1_CMD	GPT_COMPARE1	+3,3V
185	SD1_DATA2	GPT_COMPARE2	+3,3V
186	SD1_DATA3	GPT_COMPARE3	+3,3V

Table 35

6.1.4 IIC Configuration

IIC1 interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
6 / 23	CSI_DATA00 / GPIO1_IO00	SCL	+3,3V
7 / 24	CSI_DATA01 / GPIO1_IO01	SDA	+3,3V

Table 36

IIC2 interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
56 / 111 / 183	QSPI1B_DATA3 / SD4_DATA3 / GPIO1_IO02	SCL	+3,3V
55 / 110	QSPI1B_DATA2 / SD4_DATA2	SDA	+3,3V

Table 37

IIC4 interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
12 / 114 / 171	CSI_DATA06 / SD3_DATA0 / SD2_DATA1	SCL	+3,3V
13 / 124 / 168	CSI_DATA07 / SD3_DATA1 / SD2_DATA0	SDA	+3,3V

Table 38

6.1.5 Alternative UART pins tables

The following tables shows an alternative UART configuration

UART2 interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
112 / 187	GPIO1_IO06 / SD1_DATA1	UART2_TXD	+3,3V
113 / 188	GPIO1_IO07 / SD1_DATA0	UART2_RXD	+3,3V

Table 39

UART3 interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
105 / 119	QSPI1B_DATA0 / SD3_DATA7	UART3_CTS	+3,3V
106 / 120	QSPI1B_DATA1 / SD3_DATA6	UART3_RTS	+3,3V
108 / 118	QSPI1B_SS0_B / SD3_DATA5	UART3_TXD	+3,3V
109 / 121	QSPI1B_SCLK / SD3_DATA4	UART3_RXD	+3,3V

Table 40

UART4 interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
14 / 37	CSI_VSYNC / SD3_CLK	UART4_CTS	+3,3V
15 / 115	CSI_HSYNC / SD3_DATA2	UART4_RTS	+3,3V
16 / 51 / 171	CSI_PIXCLK / SD3_CMD / SD2_DATA1	UART4_TXD	+3,3V
17 / 122 / 168	CSI_MCLK / SD3_DATA3 / SD2_DATA0	UART4_RXD	+3,3V

Table 41

UART5 interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
79	KEY_ROW2	UART5_CTS	+3,3V
40	KEY_COL2	UART5_RTS	+3,3V
95	KEY_COL3	UART5_TXD_MUX	+3,3V
35	KEY_ROW3	UART5_RXD_MUX	+3,3V

Table 42

UART6 interfaces

Pin number	Pin Name on i.MX6SX	Signal reference	Voltage reference
13 / 66	CSI_DATA07 / KEY_ROW0	UART5_CTS	+3,3V
12 / 130	CSI_DATA06 / KEY_COL0	UART5_RTS	+3,3V
11 / 62 / 166	CSI_DATA05 / KEY_COL1 / SD2_DATA3	UART5_TXD_MUX	+3,3V
10 / 68 / 170	CSI_DATA04 / KEY_ROW1 / SD2_DATA2	UART5_RXD_MUX	+3,3V

Table 43

Chapter

7

7. Technical support contact

For help, write an email to:

support@engicam.com

Chapter

8

8. Useful links

http://www.nxp.com/

http://www.engicam.com/

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