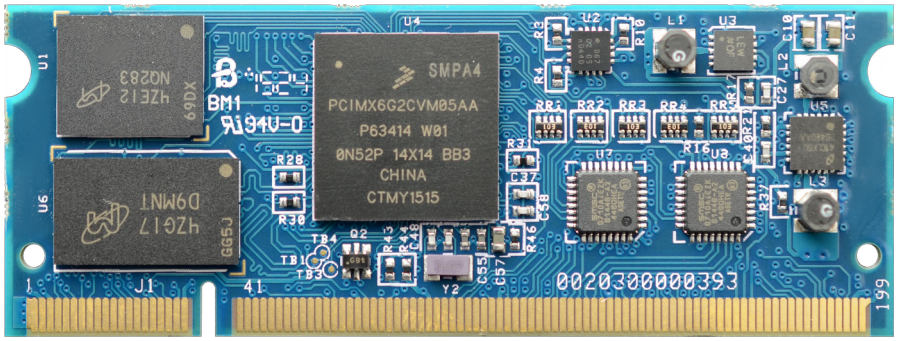
Gea M6UL HW manual 2.0.4
Getting started manual



***** REV 2.0.4 *****

DATE	REVISION	CHANGE DESCRIPTION
23/10/15	1.0.0	Release
01/12/15	1.0.1	Added pinout update
21/01/16	1.0.2	Added Reset pin informations; added power current consumption; updated Boot pins configurations
12/09/16	2.0.0	New PCB revision, added eMMC assembly option
10/10/16	2.0.1	General enhancement
28/10/16	2.0.2	Important correction on PAD CPU Reference (pinout table).for details see PCN1610-1
09/01/17	2.0.3	Electrical specifications updated
07/04/17	2.0.4	Updated ordering code

Summary

Chapter

1

1. Introduction

This Chapter gives background information on this document.

Section includes :

- ✔ **General Overview**
- ✔ **Acronyms and Abbreviations Used**
- ✔ **Document and Standard References**

1.1 Introduction

This document is created to guide users to design GEA M6UL compliant carrier board. It will focus only on the interfaces in GEA M6UL pinouts and related peripherals.

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

All examples of this document are based on GEA M6UL carrier board that is available from ENGICAM. This document also provides a collection of useful documentation, application reports, and design recommendations.

1.2 Acronyms and Abbreviations used

ABBREVIATION	EXPLANATION
ADC	Analogue to Digital Converter
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CPU	Central Processor Unit
DAC	Digital to Analogue Converter
EMI	Electromagnetic Interference, high frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
HDMI	High-Definition Multimedia Interface, combines audio and video signal
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, colour channels in common display interfaces
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
USB	Universal Serial Bus, serial interface for internal and external peripherals

1.3 Document and Standard References

1.3.1 External Industry Standard Documents

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- USB Specifications (www.usb.org).

1.3.2 NXP Documents

- IMX6ULRM
- IMX6ULCEC
- USR_Guide
- AN5170
- AN5198
- IMX6ULHDG
- MX6ULEVKHDG
- IMX6ULCE
- IMX6ULTRALITEFS
- IMX6SRSFS

1.3.3 Disclaimer

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Chapter

2

2. Mechanical data

This Chapter gives information about PCB and module's dimensions.

Section includes :

- ✔ **Assembly Top**
- ✔ **Assembly Bottom**
- ✔ **Mechanical dimensions**

2.1 Mechanical data

The i.MX6UL module has a standard SO DIMM footprint compliant with TYCO ELECTRONICS code 1473005-1 or compatible connector. The PCB dimensions is L 67.6 x W 25 x H 1 mm. The distances available on PCB under the module are from 1 to 1.5 mm

2.2 Assembly Top View

The GEA M6UL Module has a Standard SODIMM footprint where odd pins are on top (component) side and even pins are on bottom side.
In the Figure below is shown assembly and pin1 and pin 2 positions.

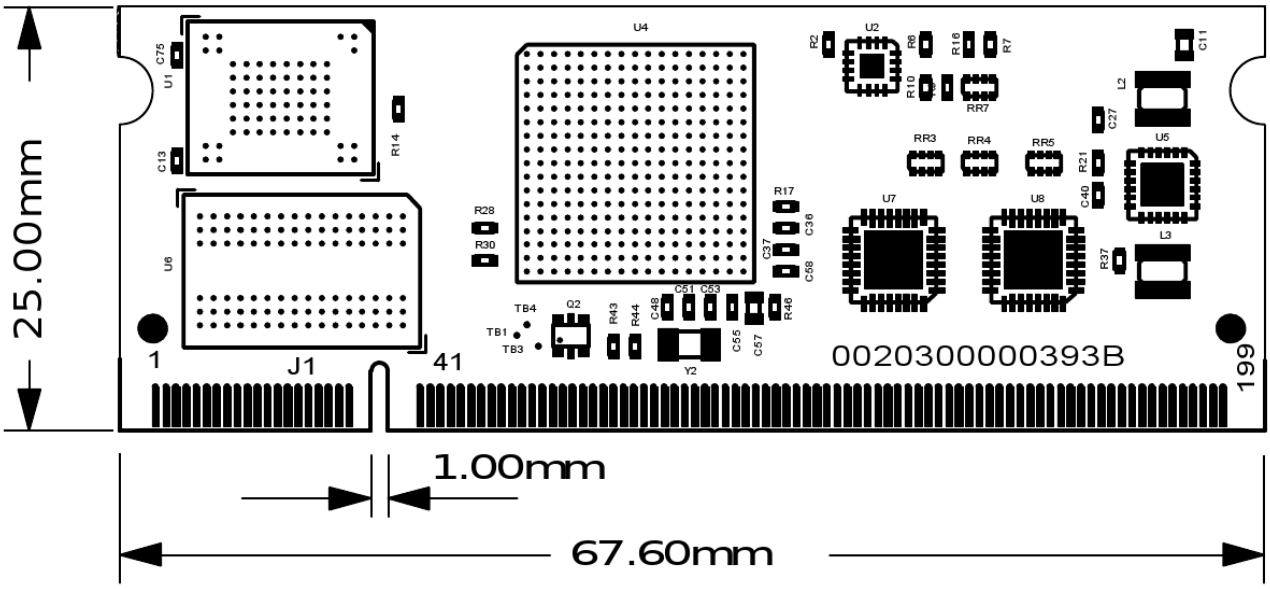

Figure 1

2.3 Assembly Bottom View

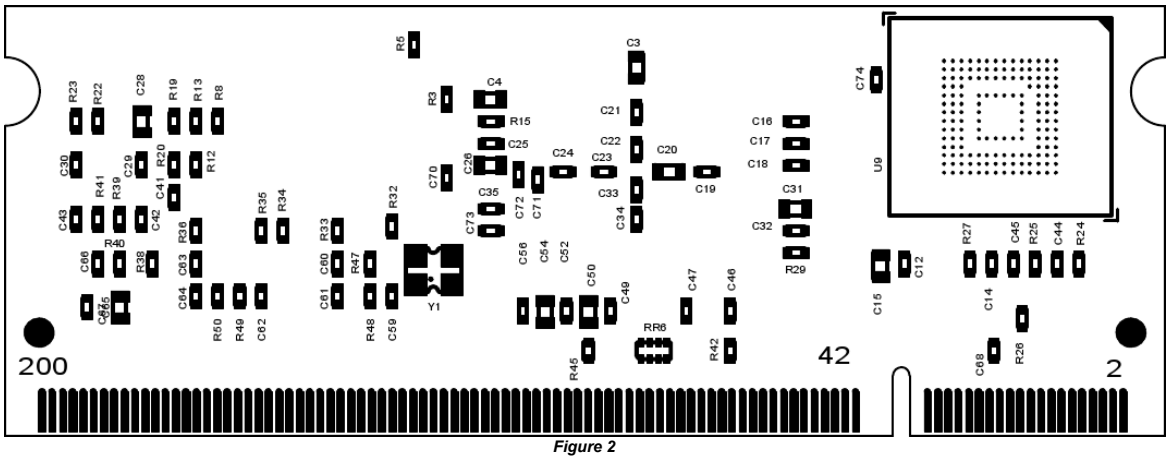

Figure 2

***Note**: in the assembly bottom picture (figure 2) it's possible to see the eMMC memory footprint and the positioning.*

Chapter

3

3. Ordering Information and Features

This Chapter gives the ordering information and technical specifications of the modules.

Section includes :

- ✔ **GEA M6UL Ordering code**
- ✔ **CPU & memory specifications**
- ✔ **Operating temperature range**

3.1 Ordering Information

In the following table some examples of orderable codes, informations and the descriptions for the modules' basic technical specifications:

Part name	Ordering Code	MPQ	Description	CPU & Memory specifications	CPU junction temperature range °C	Operating temperature range °C (excepted CPU)	Module available at least until [1)]
GEA M6UL NAND FULL	**0026820032I02C**	1	SODIMM Module GEA M6UL FULL	EDIMM i.MX6UL MCIMX6G2, 528MHz, 256MB DDR3, 256MB NAND, Dual Ethernet, Ind. Temp.	-40 to +105	-40 to +85	4 th Q - 2030
GEA M6UL NAND FULL	**0026720032I02C**	58	SODIMM Module GEA M6UL FULL		-40 to +105	-40 to +85	4 th Q - 2030
GEA M6UL NAND BASIC	**0026800032I01C**	1	SODIMM Module GEA M6UL BASIC	EDIMM i.MX6UL MCIMX6G2, 528MHz, 128MB DDR3, 256MB NAND, Single Ethernet, Ind. Temp.	-40 to +105	-40 to +85	4 th Q - 2030
GEA M6UL NAND BASIC	**0026700032I01C**	58	SODIMM Module GEA M6UL BASIC		-40 to +105	-40 to +85	4 th Q - 2030
eMMC Version	**Ordering Code**	**MPQ**	**Description**	**CPU & Memory specifications**	**CPU junction temperature range °C**	**Operating temperature range °C (excepted CPU)**	**Module available at least until [1)]**
GEA M6UL eMMC BASIC 8G	**0026800032I53C**	1	SODIMM Module GEA M6UL eMMC BASIC	EDIMM i.MX6UL MCIMX6G2, 528MHz, 512MB DDR3, 8GB eMMC, Single Ethernet, Industrial	-40 to +105	-40 to +85	4 th Q - 2030
GEA M6UL eMMC BASIC 8G	**0026700032I53C**	58	SODIMM Module GEA M6UL eMMC BASIC		-40 to +105	-40 to +85	4 th Q - 2030
GEA M6UL eMMC BASIC 4G	**0026800032E41C**	1	SODIMM Module GEA M6UL eMMC BASIC	EDIMM i.MX6UL MCIMX6G2, 528MHz, 128MB DDR3, 4GB eMMC, Single Ethernet, Extended temp.	-40 to +105	-25 to +85	4 th Q - 2030
GEA M6UL eMMC BASIC 4G	**0026700032E41C**	58	SODIMM Module GEA M6UL eMMC BASIC		-40 to +105	-25 to +85	4 th Q - 2030

Table 1

***Note**: See the structure in the following page for the description of ordering code nomenclature, characteristics and options.*

[1)] **Long Term Availability based on NXP longevity program**

The module is available with both NAND and eMMC option. The main order codes, shown in the table above, could be modified following the structure below:

MPQ	A
58	7
1	8

OPTION AVAILABLE	B
Single ethernet (BASIC)	0
Dual ethernet (FULL)	2

SOM TYPE	CCC
GEA M6UL	003

CPU TYPE RELATED TO SOM	D
-	-
-	-
G2	2
-	-

H	Reserved

G	RAM SIZE
1	128MB
2	256MB
3	512MB

F	NON VOLATILE MEMORY SPECIFICATION
0	256MB SLC NAND
1	512MB SLC NAND
4	4GB eMMC
5	8GB eMMC

E	TEMPERATURE QUALIFIER
C	-
E	Extended Temperature
I	Industrial
A	-

Ordering Code nomenclature

Chapter

4

4. Pinout

This Chapter gives the pinout informations.

Section includes :

- ✔ **Pinout overview**
- ✔ **i.MX Pad spacifications**
- ✔ **Electrical specification**

4.1 Module Pinout

The module's interface is achieved by a SO DIMM 200 position connector TYCO ELECTRONICS code 1473005-1 or compatible

Pin	Name	Pin Name on I.MX6	Primary Function Description	GPIO Capable	Voltage
1	+1V8	-	Output Power PIN	-	-
2	+1V8	-	Output Power PIN	-	-
3	GND	-	Power PIN	N	-
4	GND	-	Power PIN	N	-
5	GND	-	Power PIN	N	-
6	GPIO5_IO00	SNVS_TAMPER0	Spare GPIO	Y	+3,3V
7	GPIO5_IO01	SNVS_TAMPER1	Spare GPIO	Y	+3,3V
8	GPIO5_IO02	SNVS_TAMPER2	Spare GPIO	Y	+3,3V
9	GPIO5_IO03	SNVS_TAMPER3	Spare GPIO	Y	+3,3V
10	GPIO5_IO04	SNVS_TAMPER4	Spare GPIO	Y	+3,3V
11	GPIO5_IO07	SNVS_TAMPER7	Spare GPIO	Y	+3,3V
12	GPIO5_IO08	SNVS_TAMPER8	Spare GPIO	Y	+3,3V
13	GPIO5_IO09	SNVS_TAMPER9	Spare GPIO	Y	+3,3V
14	GPIO1_IO10	JTAG_MOD	Spare GPIO	Y	+3,3V
15	GPIO3_23 1)	LCD_DATA18	Spare GPIO	Y	+3,3V
16	GPIO3_24 3)	LCD_DATA19	Spare GPIO	Y	+3,3V
17	NC	-	-	N	-
18	+Vcoin 2)	VDD_SNVS_IN	Backup battery or RTC	-	-
19	NC	-	-	-	-
20	NC	-	-	-	-
21	NC	-	-	-	-
22	GND	-	Power PIN	N	-
23	I2C1_SCL	UART4_TX_DATA	I2C SCL Signal	Y	+3,3V
24	I2C1_SDA	UART4_RX_DATA	I2C SDA Signal	Y	+3,3V
25	TOUCH_XP	GPIO1_IO04	Touch Screen Xp (touch controller input)	-	+3,3V
26	TOUCH_XN	GPIO1_IO03	Touch Screen Xn (touch controller input)	-	+3,3V
27	TOUCH_YP	GPIO1_IO02	Touch Screen Yp (touch controller input)	-	+3,3V
28	TOUCH_YN	GPIO1_IO01	Touch Screen Yn (touch controller input)	-	+3,3V
29	NC	-	-	-	-
30	NC	-	-	-	-
31	GND	-	Power PIN	N	-
32	NC	-	-	-	-
33	ADC0_WIPER	GPIO1_IO00	Analog Input	Y	+3,3V
34	AUD_MCLK	JTAG_TMS	I2S Master Clock	Y	+3,3V
35	GPIO4_14	NAND_CE1_B	Generic GPIO	Y	+3,3V
36	GPIO4_16	NAND_DQS	Generic GPIO	Y	+3,3V

Pin	Name	Pin Name on I.MX6	Primary Function Description	GPIO Capable	Voltage
37	SD2_CD	CSI_MCLK	uSDHC2 CD Signal	Y	+3,3V
38	GPIO1_8	GPIO1_IO08	Generic GPIO	Y	+3,3V
39	GND	-	Power PIN	-	-
40	GPIO4_18	CSI_PIXCLK	Generic GPIO	Y	+3,3V
41	NC	-	-	-	-
42	NC	-	-	-	-
43	NC	-	-	-	-
44	NC	-	-	-	-
45	NC	-	-	-	-
46	NC	-	-	-	-
47	NC	-	-	-	-
48	NC	-	-	-	-
49	NC	-	-	-	-
50	NC	-	-	-	-
51	NC	-	-	-	-
52	NC	-	-	-	-
53	NC	-	-	-	-
54	NC	-	-	-	-
55	NC	-	-	-	-
56	NC	-	-	-	-
57	NC	-	-	-	-
58	NC	-	-	-	-
59	NC	-	-	-	-
60	NC	-	-	-	-
61	NC	-	-	-	-
62	GPIO3_4	LCD_RESET	Generic GPIO	Y	+3,3V
63	SPI1_MOSI	CSI_DATA06	Enhanced Configurable SPI MOSI	Y	+3,3V
64	GND	-	Power PIN	N	-
65	GPIO3_27 1)	LCD_DATA22	Generic GPIO	Y	+3,3V
66	GPIO1_25	UART3_RX_DATA	Generic GPIO	Y	+3,3V
67	NC	-	-	-	-
68	SPI1_SS0	CSI_DATA05	Enhanced Configurable SPI Chip Select	Y	+3,3V
69	NC	-	-	-	-
70	NC		-	-	-
71	GND	-	Power PIN	N	-
72	SPI1_CLK	CSI_DATA04	Enhanced Configurable SPI CLK	Y	+3,3V
73	SPI1_MISO	CSI_DATA07	Enhanced Configurable SPI MISO	Y	+3,3V
74	NC	-	-	-	-
75	NC	-	-	-	-
76	NC	-	-	-	-

Pin	Name	Pin Name on I.MX6	Primary Function Description	GPIO Capable	Voltage
77	NC	-	-	-	-
78	NC	-	-	-	-
79	GPIO1_18	UART1_CTS_B	Generic GPIO	-	-
80	nSD_BOOT 1)	-	-	-	+3,3V
81	NC	-	-	-	-
82	NC	-	-	-	-
83	NC	-	-	-	-
84	NC	-	-	-	-
85	NC	-	-	-	-
86	NC	-	-	-	-
87	NC	-	-	-	-
88	NC	-	-	-	-
89	GND	-	Power PIN	N	-
90	NC	-	-	-	-
91	NC	-	-	-	-
92	NC	-	-	-	-
93	NC	-	-	-	-
94	ETH1_TXP 4)	-	Fast Ethernet TXP signal	-	-
95	NC	-	-	-	-
96	ETH1_TXN 4)	-	Fast Ethernet TXN signal	-	-
97	ETH1_LED_10_100_KATHOD 4)	-	Led Indicator Cathode signal	-	-
98	ETH1_RXP 4)	-	Fast Ethernet RXP signal	-	-
99	ETH1_LED_ACT_ANOD 4)	-	Led indicator Anode signal	-	-
100	ETH1_RXN 4)	-	Fast Ethernet RXN signal	-	-
101	NC	-	-	-	-
102	NC	-	-	-	-
103	NC	-	-	-	-
104	NC	-	-	-	-
105	UART8_CTS	ENET2_TX_CLK	UART8 CTS signal	Y	+3,3V
106	UART8_RTS 1)	LCD_DATA23	UART8 RTS signal	Y	+3,3V
107	GND	-	Power PIN	N	-
108	UART8_TXD 3)	LCD_DATA20	UART8 TXD signal	Y	+3,3V
109	UART8_RXD 3)	LCD_DATA21	UART8 RXD signal	Y	+3,3V
110	I2C2_SDA	UART5_RXD	I2C SDA Signal	Y	+3,3V
111	I2C2_SCL	UART5_TXD	I2C SCL Signal	Y	+3,3V
112	UART2_TXD	UART2_TXD	UART2 TXD signal	Y	+3,3V
113	UART2_RXD	UART2_RXD	UART2 RXD signal	Y	+3,3V
114	I2S_DIN	JTAG_TCK	I2S Data In	Y	+3,3V
115	I2S_LRCLK	JTAG_TDO	I2S RCLK	Y	+3,3V
116	UART1_TXD	UART1_TXD	UART1 TXD signal	Y	+3,3V

Pin	Name	Pin Name on I.MX6	Primary Function Description	GPIO Capable	Voltage
117	UART1_RXD	UART1_RXD	UART1 RXD signal	Y	+3,3V
118	CAN1_TX	UART3_CTS	CAN 1 transmit signal	Y	+3,3V
119	CAN1_RX	UART3_RTS	CAN 1 receive signal	Y	+3,3V
120	CAN2_TX	UART2_CTS	CAN 2 transmit signal	Y	+3,3V
121	CAN2_RX	UART2_RTS	CAN 2 receive signal	Y	+3,3V
122	I2S_DOUT	JTAG_TRST	I2S Data Out	Y	+3,3V
123	GND	-	Power PIN	N	-
124	I2S_SCLK	JTAG_TDI	I2S SCLK	Y	+3,3V
125	DISP0_CLK	LCD_CLK	LCD interface	Y	+3,3V
126	NC	-	-	-	-
127	ETH0_TXN	-	Fast Ethernet TXN signal	-	-
128	nRESET	POR_B	Reset signal	N	+3,3V
129	ETH0_TXP	-	Fast Ethernet TXP signal	-	-
130	NC	-	-	-	-
131	ETH0_RXN	-	Fast Ethernet RXN signal	-	-
132	DISP0_CONTRAST	ENET1_RX_ER	LCD interface	Y	+3,3V
133	ETH0_RXP	-	Fast Ethernet RXP signal	-	-
134	+3V3_OUT	-	Output Power PIN	N	-
135	+3V3_OUT	-	Output Power PIN	N	-
136	NC	-	-	-	-
137	ETH0_LED_10_100_KATHOD	-	Led Indicator Cathode signal	-	-
138	NC	-	-	-	-
139	ETH0_LED_ACT_ANOD	-	Led indicator Anode signal	-	-
140	+3V3_OUT	-	Output Power PIN	-	-
141	DISP0_D17 1)	LCD_DATA17	LCD interface	Y	+3,3V
142	DISP0_D16 1)	LCD_DATA16	LCD interface	Y	+3,3V
143	DISP0_D15 1)	LCD_DATA15	LCD interface	Y	+3,3V
144	DISP0_D14 1)	LCD_DATA14	LCD interface	Y	+3,3V
145	DISP0_D13 1)	LCD_DATA13	LCD interface	Y	+3,3V
146	DISP0_D12 1)	LCD_DATA12	LCD interface	Y	+3,3V
147	DISP0_D11 1)	LCD_DATA11	LCD interface	Y	+3,3V
148	DISP0_D10 1)	LCD_DATA10	LCD interface	Y	+3,3V
149	DISP0_D9 1)	LCD_DATA09	LCD interface	Y	+3,3V
150	DISP0_D8 1)	LCD_DATA08	LCD interface	Y	+3,3V
151	DISP0_D7 1)	LCD_DATA07	LCD interface	Y	+3,3V
152	DISP0_D6 1)	LCD_DATA06	LCD interface	Y	+3,3V
153	DISP0_D5 1)	LCD_DATA05	LCD interface	Y	+3,3V
154	DISP0_D4 1)	LCD_DATA04	LCD interface	Y	+3,3V
155	DISP0_D3 1)	LCD_DATA03	LCD interface	Y	+3,3V
156	GND	-	Power PIN	N	-

Pin	Name	Pin Name on I.MX6	Primary Function Description	GPIO Capable	Voltage
157	DISP0_D2 1)	LCD_DATA02	LCD interface	Y	+3,3V
158	DISP0_D1 1)	LCD_DATA01	LCD interface	Y	+3,3V
159	DISP0_D0 1)	LCD_DATA00	LCD interface	Y	+3,3V
160	DISP0_VSYNC	LCD_VSYNC	LCD interface	Y	+3,3V
161	DISP0_HSYNC	LCD_HSYNC	LCD interface	Y	+3,3V
162	DISP0_DRDY	LCD_ENABLE	LCD interface	Y	+3,3V
163	NC	-	-	-	-
164	NC	-	-	-	-
165	NC	-	-	-	-
166	SD2_D3 3)	CSI_DATA03	uSDHC2 DAT 3 signal	Y	+3,3V
167	SD2_CMD 3)	CSI_HSYNC	uSDHC2 CMD signal	Y	+3,3V
168	SD2_D0 3)	CSI_DATA00	uSDHC2 DAT 0 signal	Y	+3,3V
169	SD2_CLK 3)	CSI_VSYNC	uSDHC2 CLK signal	Y	+3,3V
170	SD2_D2 3)	CSI_DATA02	uSDHC2 DAT 2 signal	Y	+3,3V
171	SD2_D1 3)	CSI_DATA01	uSDHC2 DAT 1 signal	Y	+3,3V
172	NC	-	-	-	-
173	NC	-	-		-
174	NC	-	-		-
175	NC	-	-		-
176	NC	-	-		-
177	NC	-	-		-
178	NC	-	-		-
179	NC	-	-		-
180	USB_H1_VBUS	USB_OTG2_VBUS	USB HOST interface	N	-
181	BOOT_MODE	BOOT_MODE	Boot from USB UART or on board Nand Flash	-	-
182	GND	-	Power PIN	N	-
183	SD1_CD	UART1_RTS_B	uSDHC1 CD Signal	Y	+3,3V
184	GPIO1_9	GPIO1_IO09	Generic GPIO - uSDHC1 WP Signal	Y	+3,3V
185	SD1_D2	SD1_DATA2	uSDHC1 DAT 2 signal	Y	+3,3V
186	SD1_D3	SD1_DATA3	uSDHC1 DAT 3 signal	Y	+3,3V
187	SD1_D1	SD1_DATA1	uSDHC1 DAT 1 signal	Y	+3,3V
188	SD1_D0	SD1_DATA0	uSDHC1 DAT 0 signal	Y	+3,3V
189	SD1_CLK	SD1_CLK	uSDHC1 CLK signal	Y	+3,3V
190	SD1_CMD	SD1_CMD	uSDHC1 CMD signal	Y	+3,3V
191	USB_OTG_ID	UART3_TX_DATA	USB on the go interface	N	-
192	USB_OTG_DP	USB_OTG1_DP	USB on the go interface	N	-
193	USB_OTG_DN	USB_OTG1_DN	USB on the go interface	N	-
194	USB_H1_DP	USB_OTG2_DP	USB HOST interface	N	-
195	USB_OTG_VBUS	USB_OTG1_VBUS	USB on the go interface	N	-
196	USB_H1_DN	USB_OTG2_DN	USB HOST interface	N	-

Pin	Name	Pin Name on I.MX6	Primary Function Description	GPIO Capable	Voltage
197	+5Vin	-	Power PIN	N	-
198	+5Vin	-	Power PIN	N	-
199	+5Vin	-	Power PIN	N	-
200	+5Vin	-	Power PIN	N	-

Table 2

[1] *Note: for the use of this pin please refer to boot option in "**Boot Mode Pin"** chapter*

[2] *Connect to Coin-Cell or Super-Cap; left floating if not use*

[3] *WARNING: **the** **peripheral SD2 (uSDHC2) is not available in the modules that mount the eMMC***

[4] ***Note:** that **Ethernet 1 is available only for FULL** versions module*

The yellow lines highlight the required minimum electrical connections in order to make the module working correctly.

4.2 What's new

Peripheral	REV B	REV A
Added memory device	**eMMC (option)**	Only NAND

Table 3

WARNING:
the** **peripheral SD2 (uSDHC2) is not available in the modules that mount the eMMC. Some peripherals, e.g. the Wi-Fi modules that use SD interface can not be used

4.3 Electrical specifications

	V Min (Volts)	V Typ (Volts)	V Max (Volts)
Vin [1]	+ 3,6 [2]	+ 5	+ 5,5
VBUS_OTG_USB, VBUS_USB	+ 4,40	+ 5	+5.35
GPIO V(oh)	+ 3,15	-	-
GPIO V(ol)	-	-	+ 0,15
GPIO V(ih)	+ 2,35		+ 3,3
GPIO V(il)	0	-	+ 1

Table 4

[1] ***This measure has done testing the module's start at the limit temperatures of -40°C and +85°C***

[2] ***Warning: the use of V Min voltage to power the module is not enough to power also the VBUS for USB peripherals***

Following, the current consumption test on module type GEA M6UL NAND BASIC, when running four different benchmarks.

Module	Test condition	Current @ V Min	Current @ V Typ	Current @ V Max
GEA M6UL NAND BASIC	Linux Sleep mode	-	15 mA	-
	Linux (only standard services running)	-	80 mA	90 mA
	QT, 2D dynamic graphic application running	-	150 mA	160 mA

Table 5

The measures have been done using U-Boot revision 2.01.

Chapter

5

5. Carrier Board Design

This Chapter gives the technical specifications for carrier board design.

Section includes :

- ✔ **Carrier Board recommendations**
- ✔ **Power signals and backup battery**
- ✔ **Serials**
- ✔ **CAN Bus**
- ✔ **Ethernet**
- ✔ **USB**
- ✔ **SDIO**
- ✔ **LCD**
- ✔ **Boot mode**
- ✔ **Audio**
- ✔ **Reset pin management**

5.1 Carrier board recommended specifications

Following we'll describe the specifications required to carrier board to avoid problems of assembly process. The module is interfaced with the carrier board through a SO-DIMM with 200 positions connector type TYCO ELECTRONICS code 1473005-1 or compatible.
For proper assembly is strongly recommended to paying attention to:

5.1.1 Planarity in finish process

Due to the technical and mechanical specifications of the connector we suggest the maximum planarity of the footprint on PCB, so we suggest a type of finish obtained by horizontal process (we suggest and use for our carrier boards a type Chemical Gold finish).

5.1.2 Planarity of PCB

Also the planarity of the entire Printed Circuit Board must be kept in check especially when the your carrier board grows in size. In this case we suggest you contact the manufacturer of PCB to understand how improve the planarity of ended board and optimize the process maintaining the electrical characteristics unchanged

Note: for further detail please refer to your SO-DIMM connector's data-sheet

5.1.3 Power Supply

It's strongly recommended that the power supply of the carrier board, which feeds the driver and control devices connected with the i.MX processor, begins to work after the initialization of the processor itself

5.2 How to power the GEA M6UL module

Please read carefully the related sections before start your power stage design. This module needs to be supply up to +5Vin power. Please refer to the table below for the power supply range specification. The power dissipated by the module in the operating mode is about 200 mA, but **the system must provide at least a power of 1A at 5V to allow the start of the module.**

In the following table are shown the module power supply pins numbering, please connect all power supply pins in order to avoid damage.

Number	Name	Primary Function Description	GPIO Capable	Voltage
197	+5Vin	Power PIN	N	-
198	+5Vin	Power PIN	N	-
199	+5Vin	Power PIN	N	-
200	+5Vin	Power PIN	N	-
3	GND	Power PIN	N	-
4	GND	Power PIN	N	-
5	GND	Power PIN	N	-
22	GND	Power PIN	N	-
31	GND	Power PIN	N	-
39	GND	Power PIN	N	-
64	GND	Power PIN	N	-
71	GND	Power PIN	N	-
89	GND	Power PIN	N	-
107	GND	Power PIN	N	-
123	GND	Power PIN	N	-
156	GND	Power PIN	N	-
182	GND	Power PIN	N	-

Table 6

The module has 5 Output power PIN usable for power source. In the table below are shown the power supply pins numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
1	+1V8	Output Power PIN	N	-
2	+1V8	Output Power PIN	N	-
134	+3V3_OUT	Output Power PIN	N	-
135	+3V3_OUT	Output Power PIN	N	-
140	+3V3_OUT	Output Power PIN	N	-

Table 7

In the following table are shown the nominal maximum rating of power output:

Power output	Max output current
+1V8	100 mA (Total)
+3V3_OUT	600 mA

Table 8

WARNING!

We recommend to add a regulator voltage for an external current greater than or equal to 600 mA, in those applications where the operating temperature range is important.

NOTE: Engicam not provide for a dissipation system, it is customer's own responsibility to evaluate the appropriate heatsink and the dissipation system depending of its own application.

For further details on the power supply please refer to "i.MX 6UL" Data Sheet and Reference Manual.

5.2.1 How to connect a backup battery

The module allows the use of lithium rechargeable battery or supercapacitor as backup battery.
The connection with module is obtained by connecting directly the backup battery to the +Vcoin signal (pin 18 floating if not used).

The consumption of the pin is given by NXP for a maximum of 300uA

Note: *The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.*

Note: *The module is already designed to manage the charge of backup battery.*

For further details on the power supply please refer to "i.MX 6UL" Data Sheet and Reference Manual.

5.3 How to connect two 3-wire RS232 serial port

In this section is shown how to use the UART1 and UART2 as 3-wire RS232 serial ports.

In the following table are shown the UART1 and UART2 pins numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
112	UART2_TXD	UART2 TXD signal	Y	+3,3V
113	UART2_RXD	UART2 RXD signal	Y	+3,3V
116	UART1_TXD *	UART1 TXD signal	Y	+3,3V
117	UART1_RXD *	UART1 RXD signal	Y	+3,3V

Table 9

The signal on the module's UART pins are 3.3V logic level, this can not be connected directly to a RS232 device like a PC Serial port, the use of a transceivers on the base board is mandatory in order to avoid module damage.

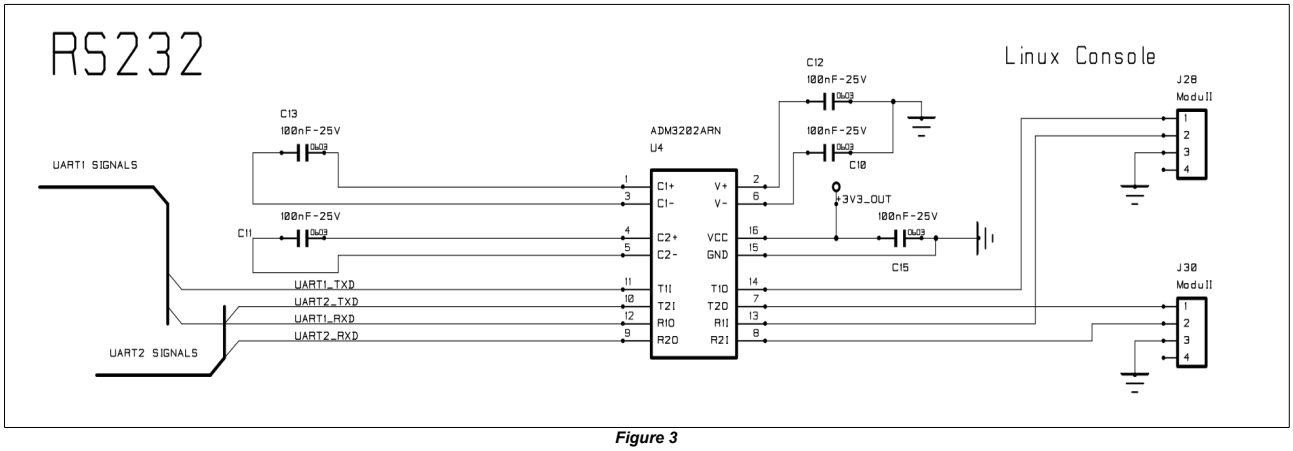

Figure 3

In this example an ADM3202ARN IC from Analog Device is used like transceiver for both UART without any control signal. In case RTS and CTS are need, a transceiver must be used for this signals.

When Linux is installed on a module, UART1 is used like console. The default communications settings is shown in the table below.

Linux console default settings	
Baud rate	115200
Data length	8 bit
Parity	none
Stop	1bit

Table 10

* **Note**: *the UART1 is used as Linux Console*

5.4 How to connect a RS485 serial port

In this chapter is shown how an RS485 serial port can be connected to the module. In the figure below is shown how UART3 is used to connect to a RS485 transceiver on the starter kit. The figure shows UART3 connection but you can consider that also UART 4 & 5 can be used to connect a RS485 transceiver.

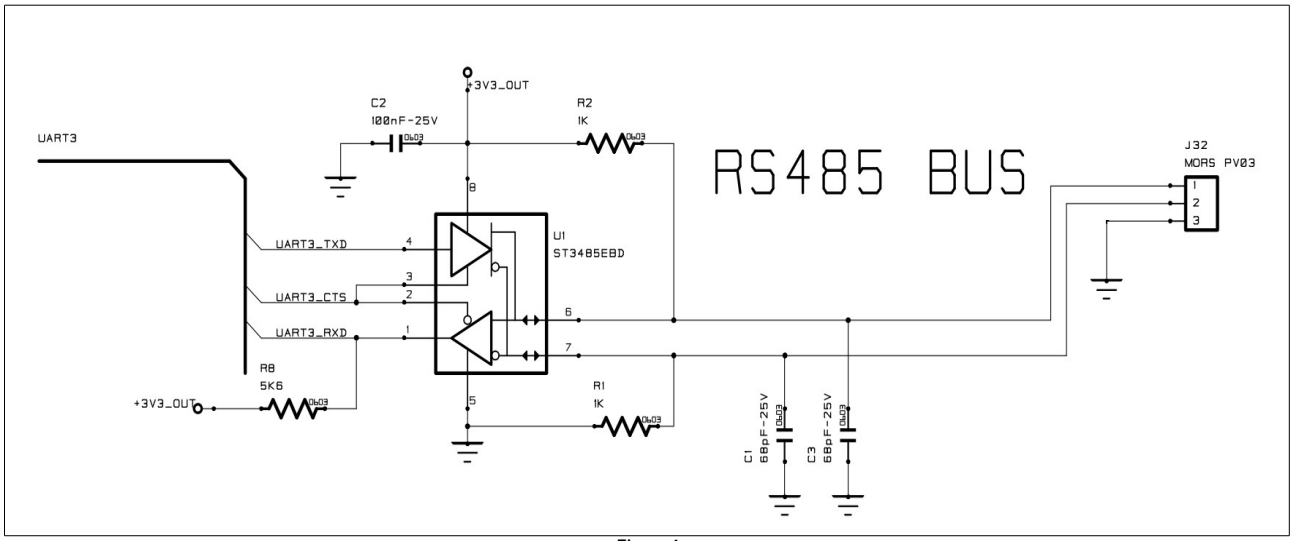

Figure 4

The pins involved in this RS485 communication example are listed in the following table.

Number	Name	Primary Function Description	GPIO Capable	Voltage
105	UART8_CTS	UART8 CTS signal	Y	+3,3V
106	UART8_RTS	UART8 RTS signal	Y	+3,3V
108	UART8_TXD	UART8 TXD signal	Y	+3,3V
109	UART8_RXD	UART8 RXD signal	Y	+3,3V

Table 11

5.5 How to connect CAN BUS interfaces

In this chapter is described how CAN bus transceiver can be connected to a module. In the figure below is shown how CAN bus1 and 2 are connected in the evaluation board. Both CAN buses have been implemented.

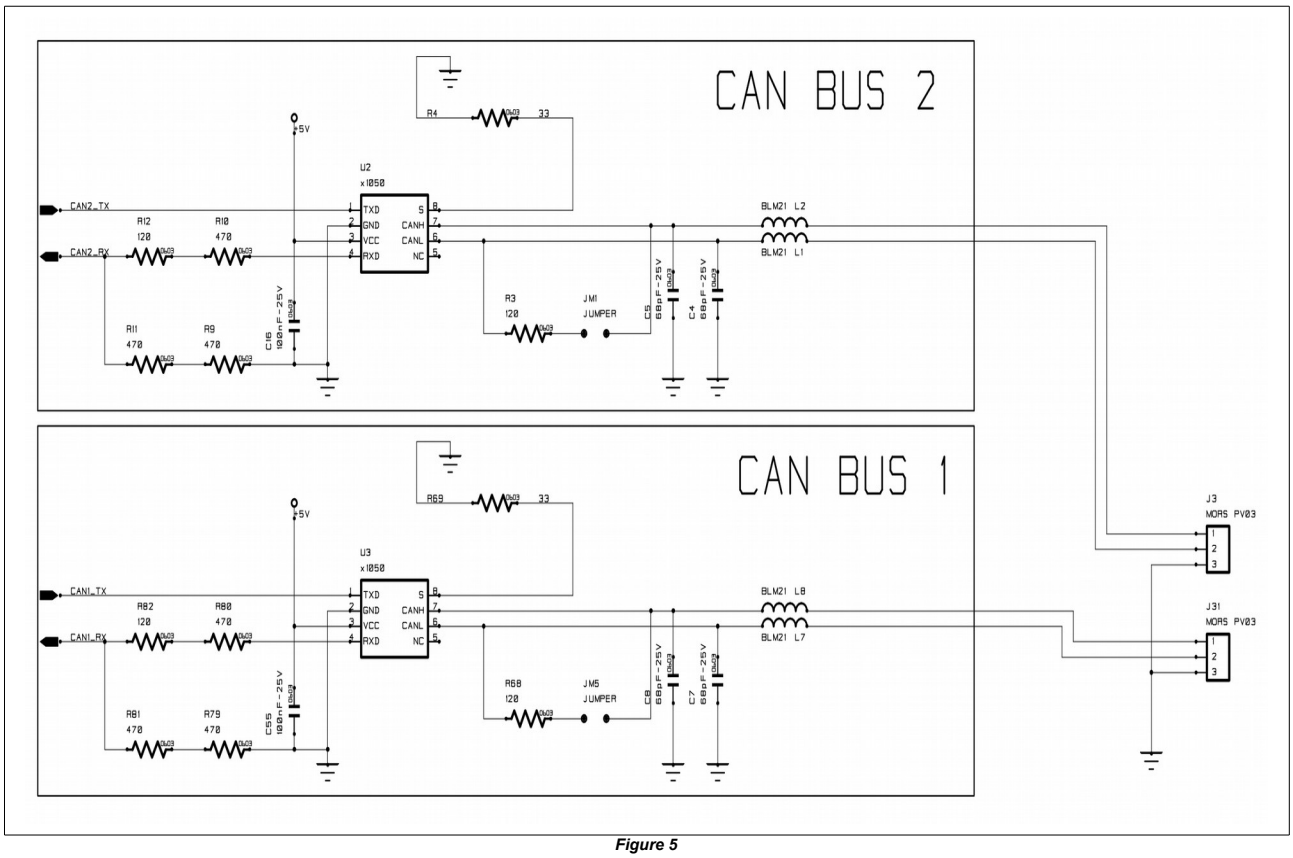

Figure 5

The following table describes the pins' numbering in the main connector involved in the CAN interface

Number	Name	Primary Function Description	GPIO Capable	Voltage
118	CAN1_TX	CAN 1 transmit signal	Y	+3,3V
119	CAN1_RX	CAN 1 receive signal	Y	+3,3V
120	CAN2_TX	CAN 2 transmit signal	Y	+3,3V
121	CAN2_RX	CAN 2 receive signal	Y	+3,3V

Table 12

The Jumpers JM1, JM5 are used to close the load of the CAN Bus to 120 Ω.

5.6 How to design the Ethernet interface

The NXP i.MX6UL Ethernet Media Access Controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE standard 802.3™ networks. The 10-Mbps and 100-Mbps RMII Ethernet physical interfaces is supported. In the figure is shown how to connect the Ethernet interface to module.

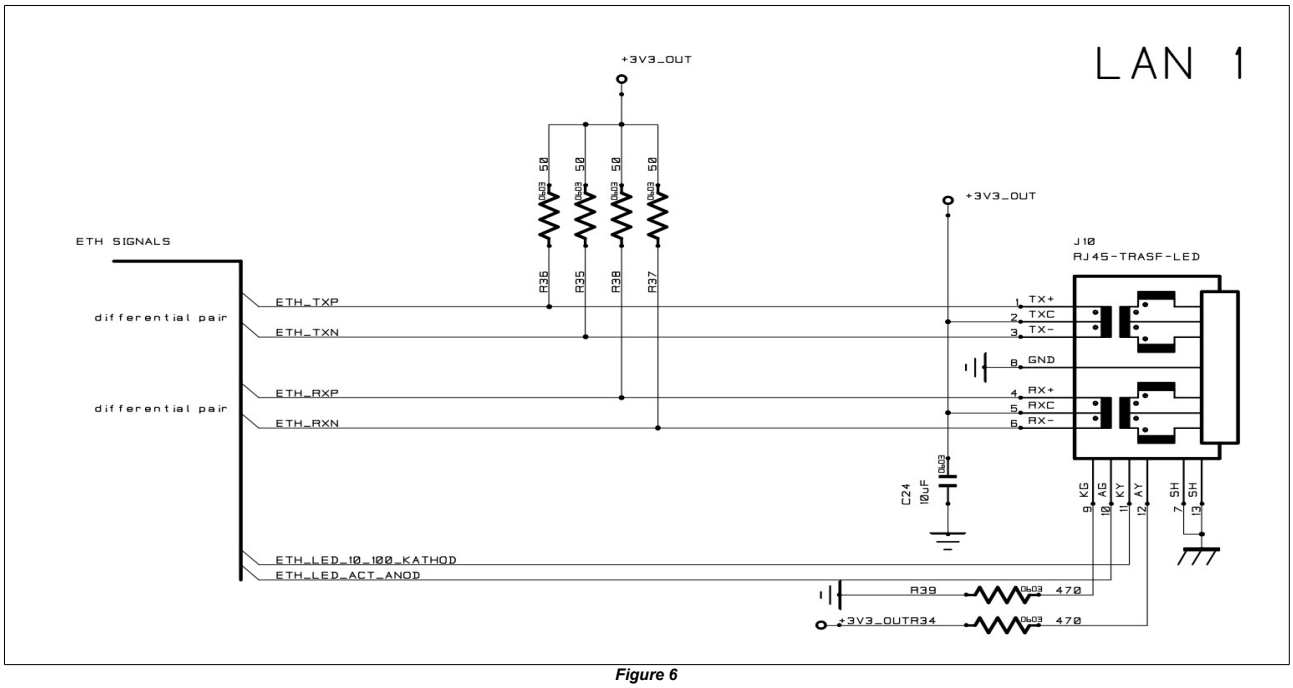

Figure 6

In the table below are listed all Ethernet signals of the module:

Number	Name	Primary Function Description	GPIO Capable	Voltage
127	ETH0_TXN	Fast Ethernet TXN signal	-	+3,3V
129	ETH0_TXP	Fast Ethernet TXP signal	-	+3,3V
131	ETH0_RXN	Fast Ethernet RXN signal	-	+3,3V
133	ETH0_RXP	Fast Ethernet RXP signal	-	+3,3V
137 *	ETH0_LED_10_100_KATHOD	Led Indicator Cathode signal	-	+3,3V
139 *	ETH0_LED_ACT_ANOD	Led indicator Anode signal	-	+3,3V

Table 13

WARNING: These pins are available only for **GEA M6UL FULL** series

Number	Name	Primary Function Description	GPIO Capable	Voltage
96	ETH1_TXN	Fast Ethernet TXN signal	-	+3,3V
94	ETH1_TXP	Fast Ethernet TXP signal	-	+3,3V
100	ETH1_RXN	Fast Ethernet RXN signal	-	+3,3V
98	ETH1_RXP	Fast Ethernet RXP signal	-	+3,3V
97 *	ETH1_LED_10_100_KATHOD	Led Indicator Cathode signal	-	+3,3V
99 *	ETH1_LED_ACT_ANOD	Led indicator Anode signal	-	+3,3V

Table 14

* ***Note:*** If not used, this pin must be left floating.

5.6.1 Component Placement considerations

Components placement can affect signal quality, emissions and can decrease EMI problems.

1. If the magnetics are a discrete component than the distance from the connector RJ45 should be kept to under 25mm of separation.
2. To decrease EMI problems the distance between magnetics and Phy should be at least 25mm or greater to isolate the PHY from magnetics.
3. The distance between Phy and RJ45 connector should always be within 200 mm.
4. The differential transmit pair should be keep at least 25mm from the edge of PCB up to the magnetics. If the magnetics are integrated into RJ45 the differential pair should be routed to the back of integrated magnetics RJ45 connector , away from the board of PCB.
5. The 49.9 ohm pull-up resistors on the differential lines should be placed within 10 mm of the Phy device
6. The signals RX & TX should be independently matched in length to within 6mm

See following figure

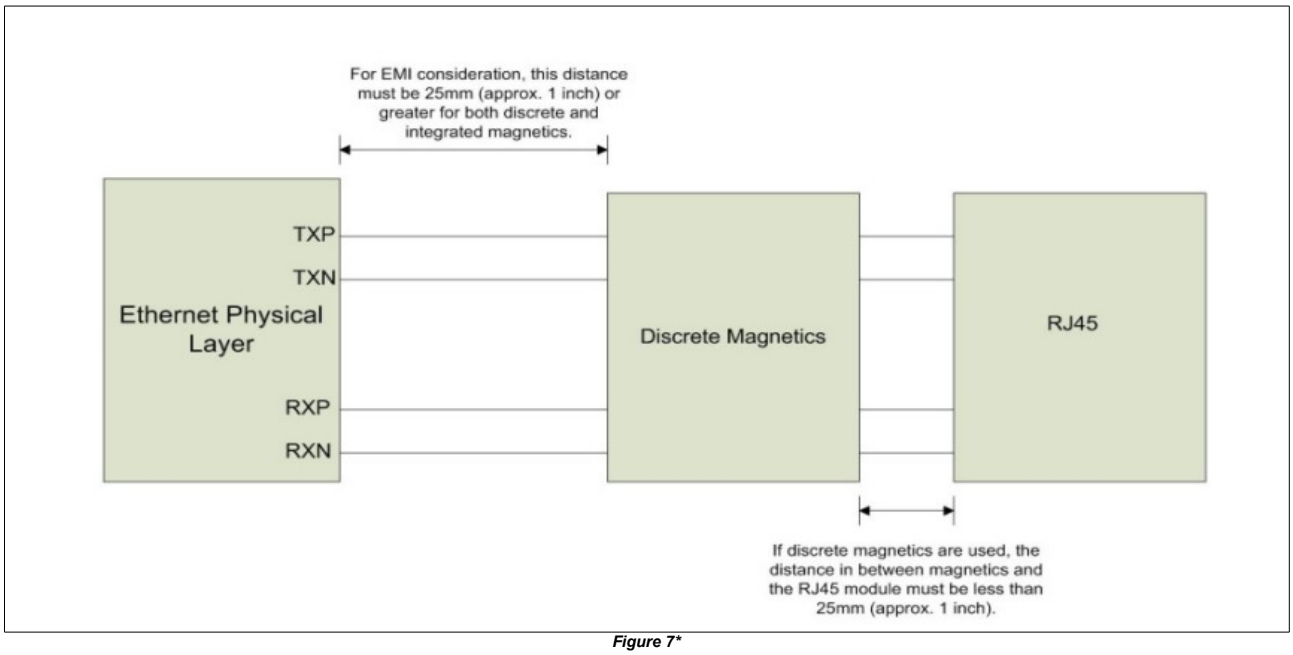

Figure 7*

The PHY used in the module is the ***SMSC LAN8710***.
Please for more information refer to the ***SMSC Ethernet Physical Layer Layout Guidelines***.

For a list of magnetics selected to operate with the SMSC LAN8710, please refer to the Application note ***AN 8-13 Suggested Magnetics.***

WARNING:
The second **LAN8710** is **assembled only** in the module **FULL** version

*** this is the figure 2.3 from SMSC Ethernet Physical Layer Layout Guidelines**

5.6.2 Cable Transient Event and PHY Protection

Cable transient events are + and - DC surges that are induced across the transformer onto the PHY side of the TX+/- and RX+/- signals as shown in figure below. The PHY side of the transformer should not contain any DC component other than the typical 3.3V pull-up on the center tap of the transformer for analog signal biasing. Especially in POE applications, there are two main reasons why cable transient events occur, negative rail PSE switching, and hot unplug/plug-in events.

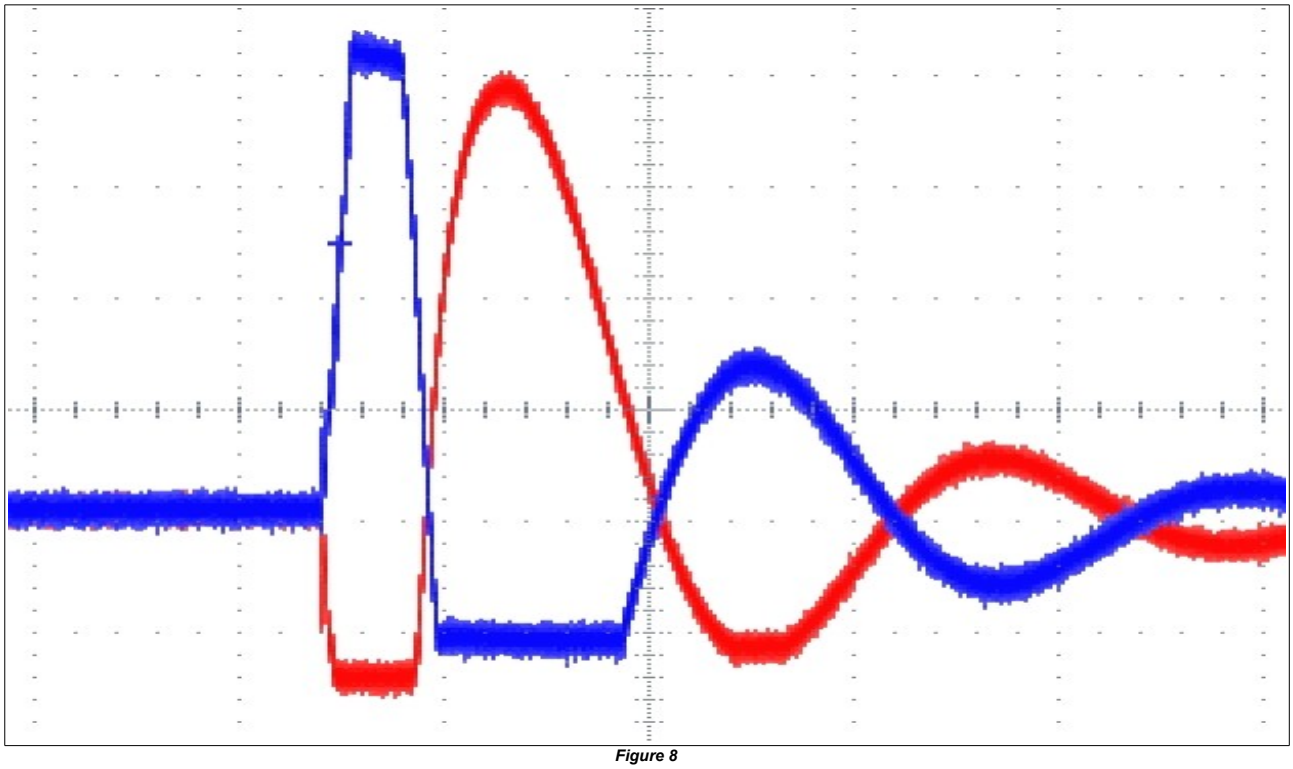

Figure 8

Transient observer on the PHY side of Eth Magnetics

Scale X = 1uS/div

Scale Y = 5V/div

Note: *for further details about Cable transient events please refers to file AN1718 of SMSC*

5.6.3 Phy Ethernet

When using an SMSC device, for each application an external transient protection is recommended , especially when the POE is used, as shown in figure below. The schematic shows an example of a TVS suppression solution. This solution couples the energy differentially into the two TVS diodes on each differential pair. For cases when the transient is across the TX+/- pair in the figure below, the voltage is clamped at a value equivalent to the forward bias voltage across D1, plus the zener voltage of D2. This transient voltage must be clamped at a voltage no **greater than 5V**. D3 and D4 act the same way when the transient is across the RX+/- differential pair. The total capacitance seen by each differential pair must not exceed 50pF (25pF single ended).

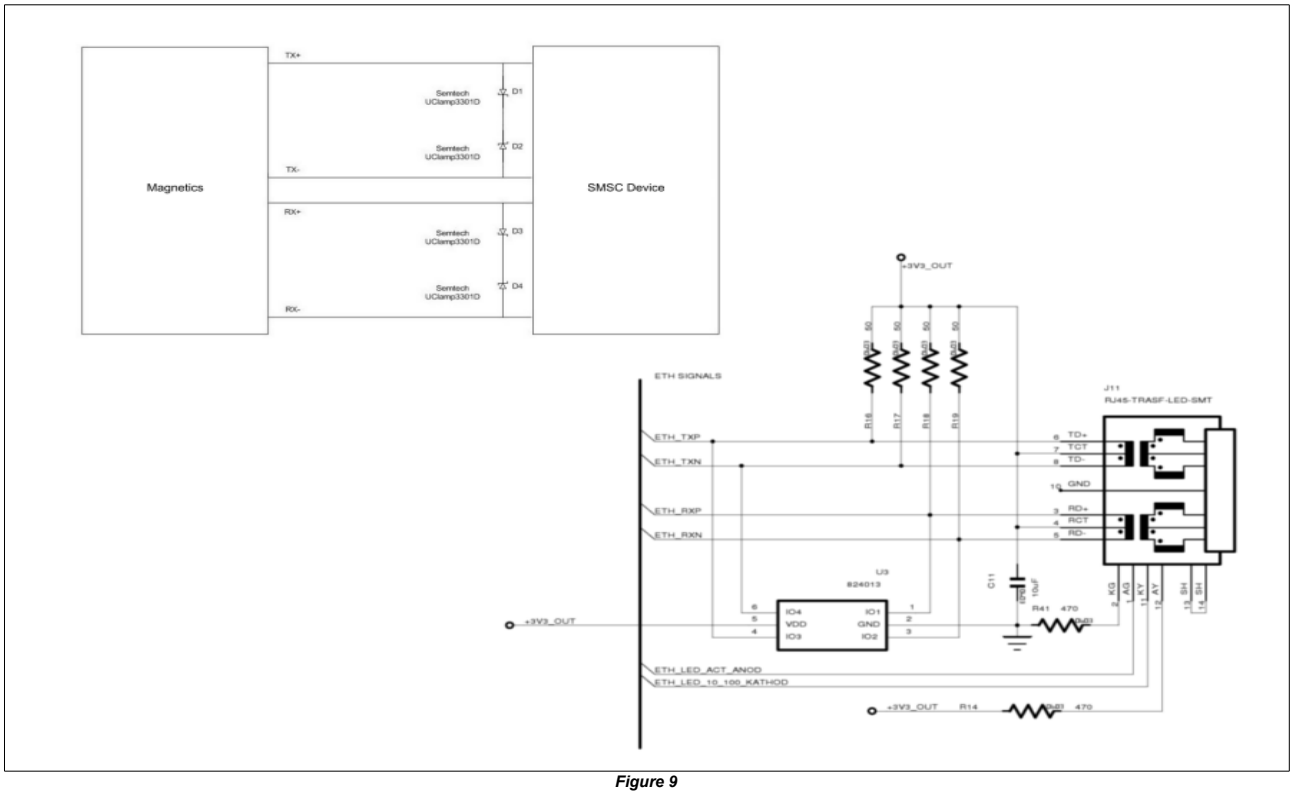

Figure 9

Recommended by ENGICAM:

Diode array TVS, 4 CH, ESD, 3.3V Wurth Elektronik 824013

Note: *for further details about PHY Protection please reffers to file AN1718 of SMSC*

5.7 USB interface

5.7.1 How to connect the USB OTG interface

The NXP i.MX6UL USB module provides high performance USB On-The-Go (up to 480Mbps), compatible with the USB 2.0 specification. An OTG HS PHY is also integrated so no external OTG PHY is needed on the baseboard. In the figure is shown how the MINI-AB USB/OTG connector is powered and connected in the evaluation board. In the following table are listed all USB/OTG signal of mail connector.

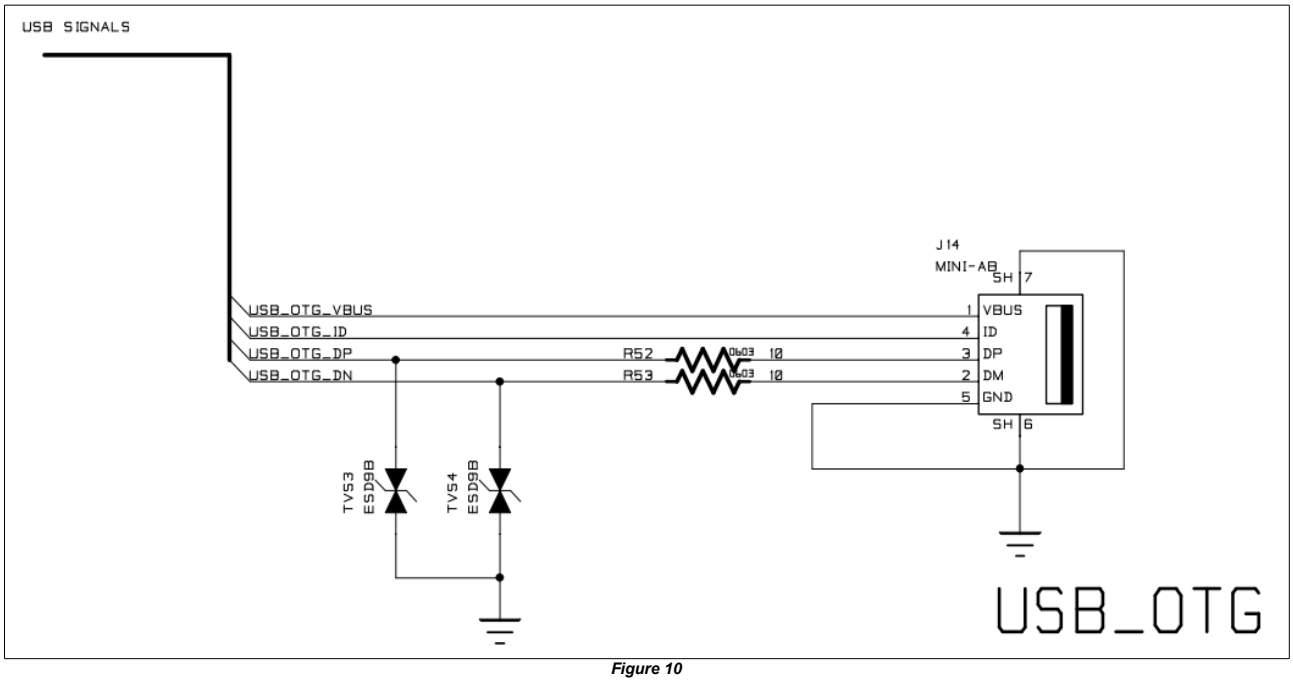

Figure 10

Number	Name	Primary Function Description	GPIO Capable	Voltage
195	USB_OTG_VBUS *	USB on the go interface	N	-
192	USB_OTG_DP	USB on the go interface	N	-
191	USB_OTG_ID	USB on the go interface	N	-
193	USB_OTG_DN	USB on the go interface	N	-

Table 15

**** Note: The USB_OTG_VBUS is an INPUT power signal. It must be connected to +5V***

In the following figures there are shown two different ways to connect the USB OTG interface that may be used to work as either a host or a device.

Use of the USB OTG port as a Host with its own dedicated supply. The ID signal is forced to GND

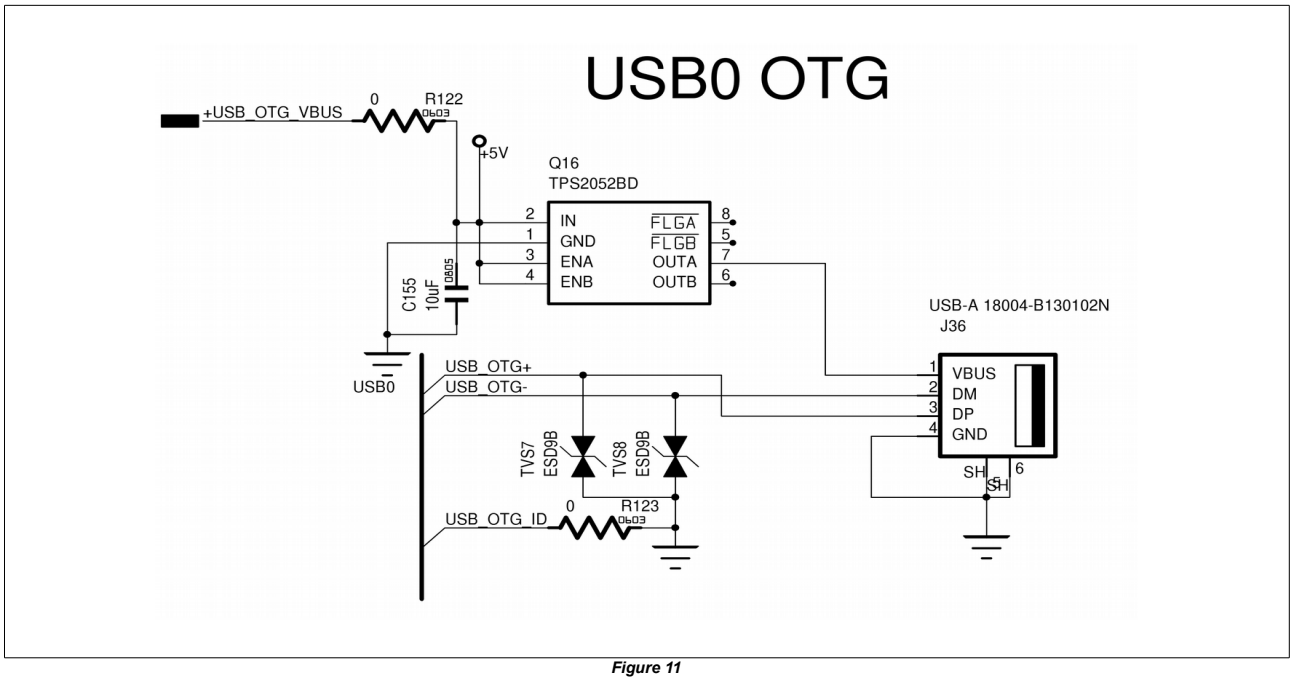

Figure 11

Use of the USB OTG port as Device or as Host depending on the status of the ID signal that is used also to enable the power supply.

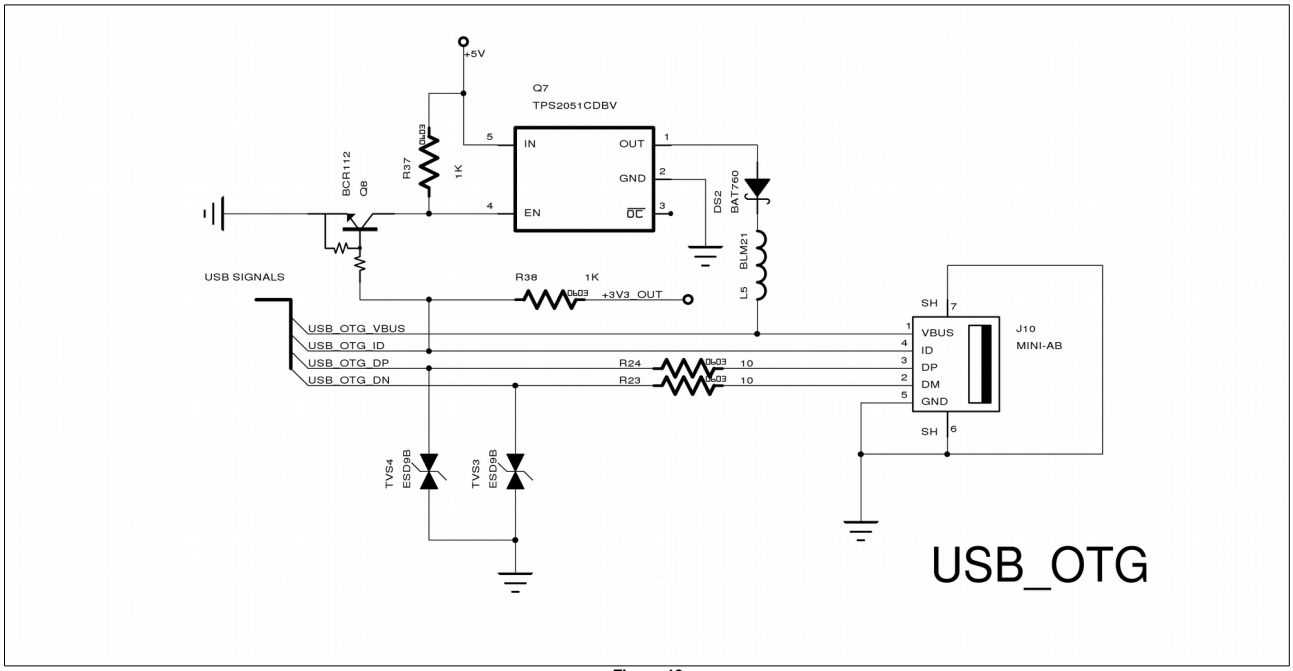

Figure 12

5.7.2 How to connect the USB host interface

The module provides one port for USB host interface. In the figure is shown how to connect this port to the Module.

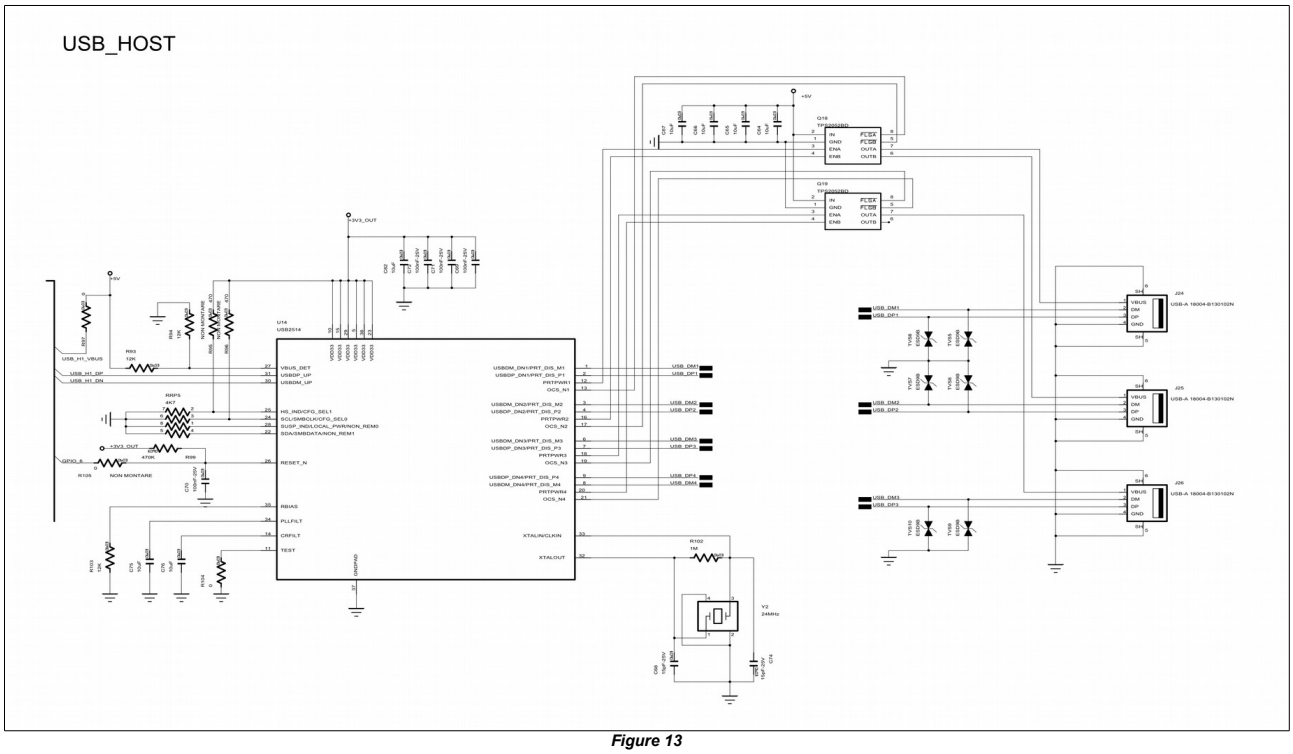

Figure 13

Engicam's evaluation board is equipped with an USB HUB to multiply the USB port available on module, if only one port is needed it's possible to connect it as one of the four output ports of the HUB output directly to module on pin 194-196 of the main connector.

Number	Name	Primary Function Description	GPIO Capable	Voltage
180	USB_H1_VBUS *	USB HOST interface	N	-
194	USB_HI_DP	USB HOST interface	N	-
196	USB_H1_DN	USB HOST interface	N	-

Table 16

**** Note: The USB_H1_VBUS is an INPUT power signal. It must be connected to +5V***

5.8 How to connect the SD CARD interface

The NXP i.MX6UL Ultra Secured Digital Host Controller (uSDHC) provides the interface between the host system and MMC/SD/SDIO/CE-ATA cards, including cards with reduced size or mini cards. The module include this features and in the figure is shown how the Micro SD Card connector is connected to GEA Module in the evaluation board. The uSDHC signal of the module's main connector are listed in table below.

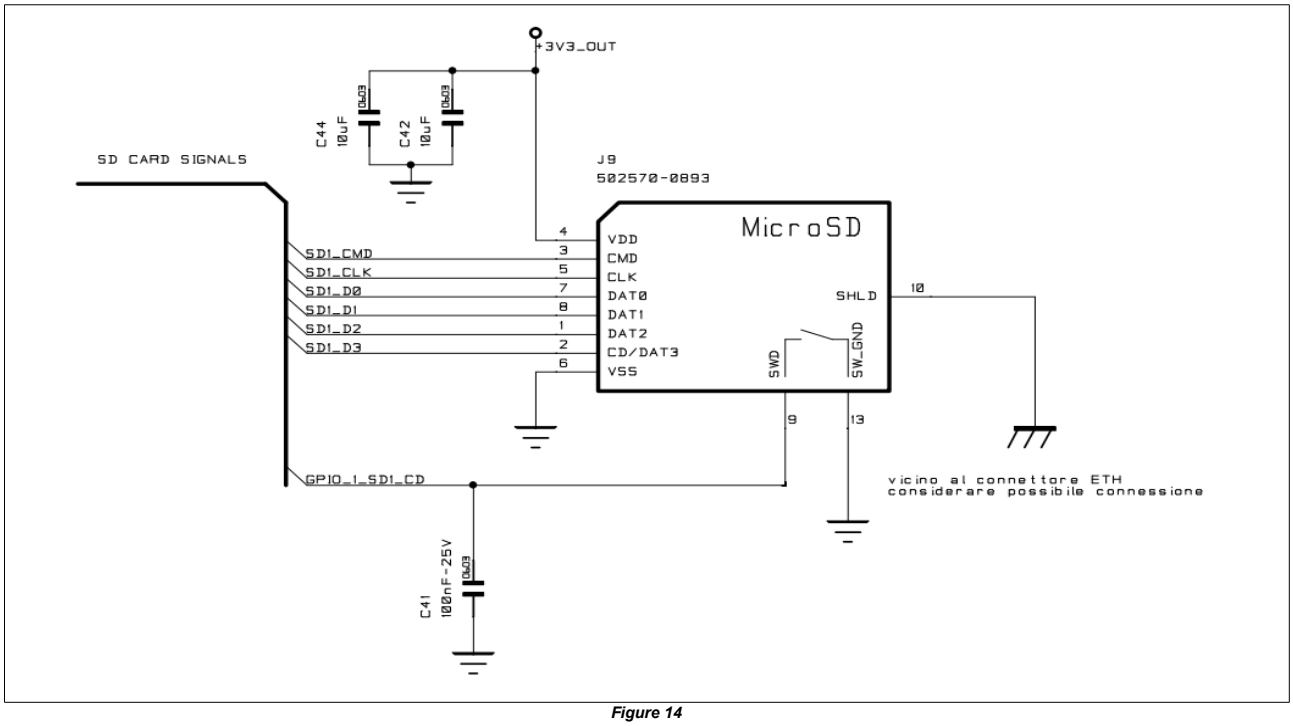

Figure 14

Number	Name	Primary Function Description	GPIO Capable	Voltage
183	SD1_CD	uSDHC1 CD Signal	Y	+3,3V
188	SD1_DAT0	uSDHC1 DAT 0 signal	Y	+3,3V
187	SD1_DAT1	uSDHC1 DAT 1 signal	Y	+3,3V
185	SD1_DAT2	uSDHC1 DAT 2 signal	Y	+3,3V
186	SD1_DAT3	uSDHC1 DAT 3 signal	Y	+3,3V
189	SD1_CLK	uSDHC1 CLK signal	Y	+3,3V
190	SD1_CMD	uSDHC1 CMD signal	Y	+3,3V

Table 17

5.9 How to connect an LCD display

The evaluation board is equipped with one RGB data port, this interface contains RGB data of 18 bit, pixel clock.
Following are reported the schematic interface with parallel URT and the map of signals.

Number	Name	Primary Function Description	GPIO Capable	Voltage
125	DISP0_CLK	LCD interface	Y	+3,3V
141	DISP0_D17	LCD interface	Y	+3,3V
142	DISP0_D16	LCD interface	Y	+3,3V
143	DISP0_D15	LCD interface	Y	+3,3V
144	DISP0_D14	LCD interface	Y	+3,3V
145	DISP0_D13	LCD interface	Y	+3,3V
146	DISP0_D12	LCD interface	Y	+3,3V
147	DISP0_D11	LCD interface	Y	+3,3V
148	DISP0_D10	LCD interface	Y	+3,3V
149	DISP0_D9	LCD interface	Y	+3,3V
150	DISP0_D8	LCD interface	Y	+3,3V
151	DISP0_D7	LCD interface	Y	+3,3V
152	DISP0_D6	LCD interface	Y	+3,3V
153	DISP0_D5	LCD interface	Y	+3,3V
154	DISP0_D4	LCD interface	Y	+3,3V
155	DISP0_D3	LCD interface	Y	+3,3V
157	DISP0_D2	LCD interface	Y	+3,3V
158	DISP0_D1	LCD interface	Y	+3,3V
159	DISP0_D0	LCD interface	Y	+3,3V
160	DISP0_VSYNC	LCD interface	Y	+3,3V
161	DISP0_HSYNC	LCD interface	Y	+3,3V
162	DISP0_DRDY	LCD interface	Y	+3,3V

Table 18

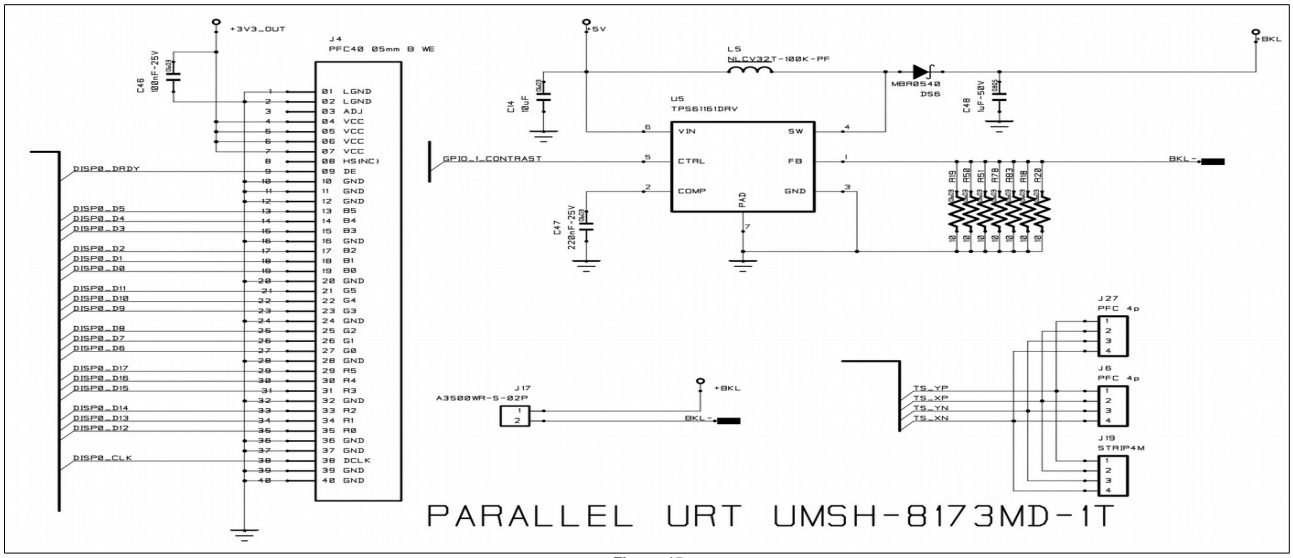

Figure 15

5.9.1 Connection map for 18 bit TFT only

The following map represent the connection mode applied to 18 bit TFT display
For every connection the colour controlled is joined

Number	Name	18 bit TFT connections
159	DISP0_D0	BLU 0
158	DISP0_D1	BLU 1
157	DISP0_D2	BLU 2
155	DISP0_D3	BLU 3
154	DISP0_D4	BLU 4
153	DISP0_D5	BLU 5
152	DISP0_D6	GREEN 0
151	DISP0_D7	GREEN 1
150	DISP0_D8	GREEN 2
149	DISP0_D9	GREEN 3
148	DISP0_D10	GREEN 4
147	DISP0_D11	GREEN 5
146	DISP0_D12	RED 0
145	DISP0_D13	RED 1
144	DISP0_D14	RED 2
143	DISP0_D15	RED 3
142	DISP0_D16	RED 4
141	DISP0_D17	RED 5

Table 19

5.10 Boot Mode Pin

Boot mode pin determines how the module boot. The following table listed the possible options of the boot mode:

BOOT_MODE	Action
0	Boot from memory devices
1	Boot from USB OTG

Table 20

The boot from USB OTG is usually used for the boot loader deploy.

In the figure is shown the boot section scheme. The standard mode expected booting from a memory device. Closing JM2 corresponds to put at logical 1 (high) the boot mode pin to boot from USB OTG.

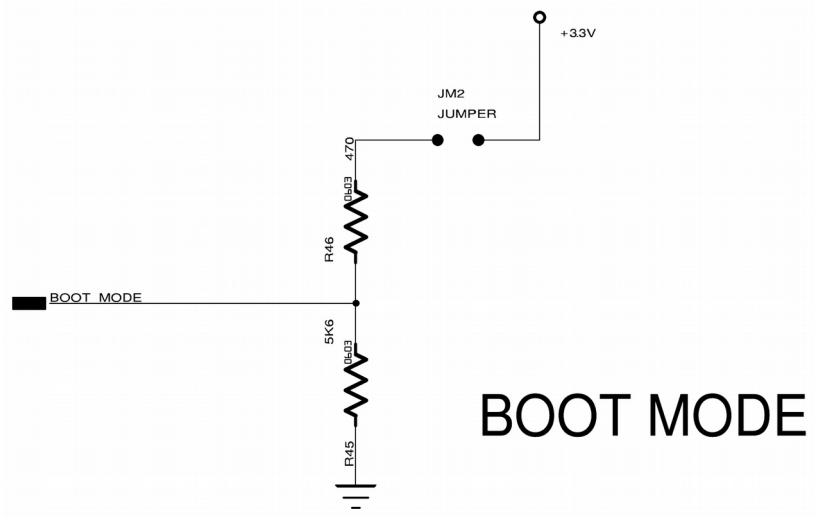

Figure 21

In Table below is listed the boot mode Pin numbering.

Number	Name	Primary Function Description	GPIO Capable	Voltage
181	BOOT_MODE	Boot from USB/UART or Memory device	N	+3,3V

Table 21

In the evaluation board we set-up all the configurations for bootstrap from memory device, NAND, eMMC or SD card.

In the figure below is shown the boot configurations available, from **memory devices**, settings the nSD_BOOT.signal.

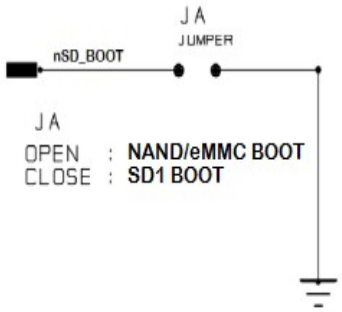

Figure 22

The figure above shows the implementation of the boot options applied to a generic carrier board. The signal used to configure the boot option on the ENGICAM EVABOARD is named EIM_DA7 (pin 80, nSD_BOOT signal on GEA M6UL) which is pulled up with a 12KOhm resistor on the module.
In the standard condition, the signal in the evaluation board is setting to boot from the module's internal memory devices (NAND or eMMC) jumper left open; the boot from the SD card is achieved simply closing the jumper.

Following, how to implement the signals logical level for a custom starting sequence.

The first sequence is already implemented in the module, nSD_BOOT signal left floating or pulled up.

BOOT from Internal Module's Memory Device		
Pin Number	**EVABOARD Signal**	**LOGIC LEVEL**
80	nSD_BOOT	1

Table 22

Setting the nSD_BOOT signal to **high logical level**:

- if module is equipped with NAND, the boot run from NAND
- if module is equipped with eMMC, the boot run from eMMC

The NAND and eMMC **can NOT** coexist in the module**.**

The choice of booting from SD1 means short-cutting the jumper A in the evaluation (or carrier) board. It's possible to have the same effect by pulling down the signal nSD_BOOT.

BOOT FROM SD1 Device		
Pin Number	**EVABOARD Signal**	**LOGIC LEVEL**
80	nSD_BOOT	0

Table 23

Whatever starting sequence is choosing consider that the pin 80 of the main connector is used to the boot configuration.

***WARNING**:*
remember that the peripheral SD2 can not be used in the modules that mount the eMMC

Note: for using of any customized boot options please refer also to the NXP i.MX6UL reference manual

5.10.1 Boot Signals Management

Following are shown the signals you must consider during the boot sequence:

Signal	SODIMM Pin number	Status on Reset (*Mandatory*)	PIN constrained on Module	Boot Config Signal	Boot eFUSE Descriptions
UART8_RTS	106	Floating	10K Ohm Pull Down	BOOT_CFG4[7]	
GPIO3_27	65	Floating	10K Ohm Pull Down	BOOT_CFG4[6]	
GPIO3_23	15	Floating	10K Ohm Pull Down	BOOT_CFG4[2]	
DISP0_D17	141	Floating	10K Ohm Pull Down	BOOT_CFG4[1]	
DISP0_D16	142	Floating	10K Ohm Pull Down	BOOT_CFG4[0]	
DISP0_D15	143	Floating	10K Ohm Pull Down	BOOT_CFG2[7]	
DISP0_D14	144	Floating	10K Ohm Pull Down	BOOT_CFG2[6]	
DISP0_D13	145	Floating	10K Ohm Pull Down	BOOT_CFG2[5]	
DISP0_D12	146	Floating	10K Ohm Pull Down	BOOT_CFG2[4]	
DISP0_D11	147	Floating	10K Ohm Pull Down	BOOT_CFG2[3]	
DISP0_D10	148	Floating	10K Ohm Pull Down	BOOT_CFG2[2]	
DISP0_D9	149	Floating	10K Ohm Pull Down	BOOT_CFG2[1]	
DISP0_D8	150	Floating	10K Ohm Pull Down	BOOT_CFG2[0]	
DISP0_D7	151	Floating	-	BOOT_CFG1[7]	
DISP0_D6	152	Floating	-	BOOT_CFG1[6]	
DISP0_D5	153	Floating	12K Ohm Pull Down	BOOT_CFG1[5]	
DISP0_D4	154	Floating	-	BOOT_CFG1[4]	
DISP0_D3	155	Floating	10K Ohm Pull Down	BOOT_CFG1[3]	
DISP0_D2	157	Floating	10K Ohm Pull Down	BOOT_CFG1[2]	
DISP0_D1	158	Floating	10K Ohm Pull Down	BOOT_CFG1[1]	
DISP0_D0	159	Floating	10K Ohm Pull Down	BOOT_CFG1[0]	

Table 24

The NXP documentation declares the above signals as BOOT_CFG signals but no other information (function and reset status) is currently given about them.
Basing on the Engicam test result we currently suggest to leave all these signals floating during reset status and **it's strongly recommended to consult the NXP's documentation before starting the carrier board design.**

WARNING:

The BOOT_CFG4 signals are used also to configure the boot from serial ROM, please always refer to the NXP's documentations to design and configure the listed BOOT_CFG signals of your own board

5.11 How to connect the Audio Interface

The evaluation board is equipped with the low-power stereo codec, NXP SGTL5000, that includes headphones and is designed to provide a comprehensive audio solution for portable products that require line-in, mic-in, line-out, headphone-out and digital I/O.

The figure shows how the device interface is connected to the module using the I2S BUS

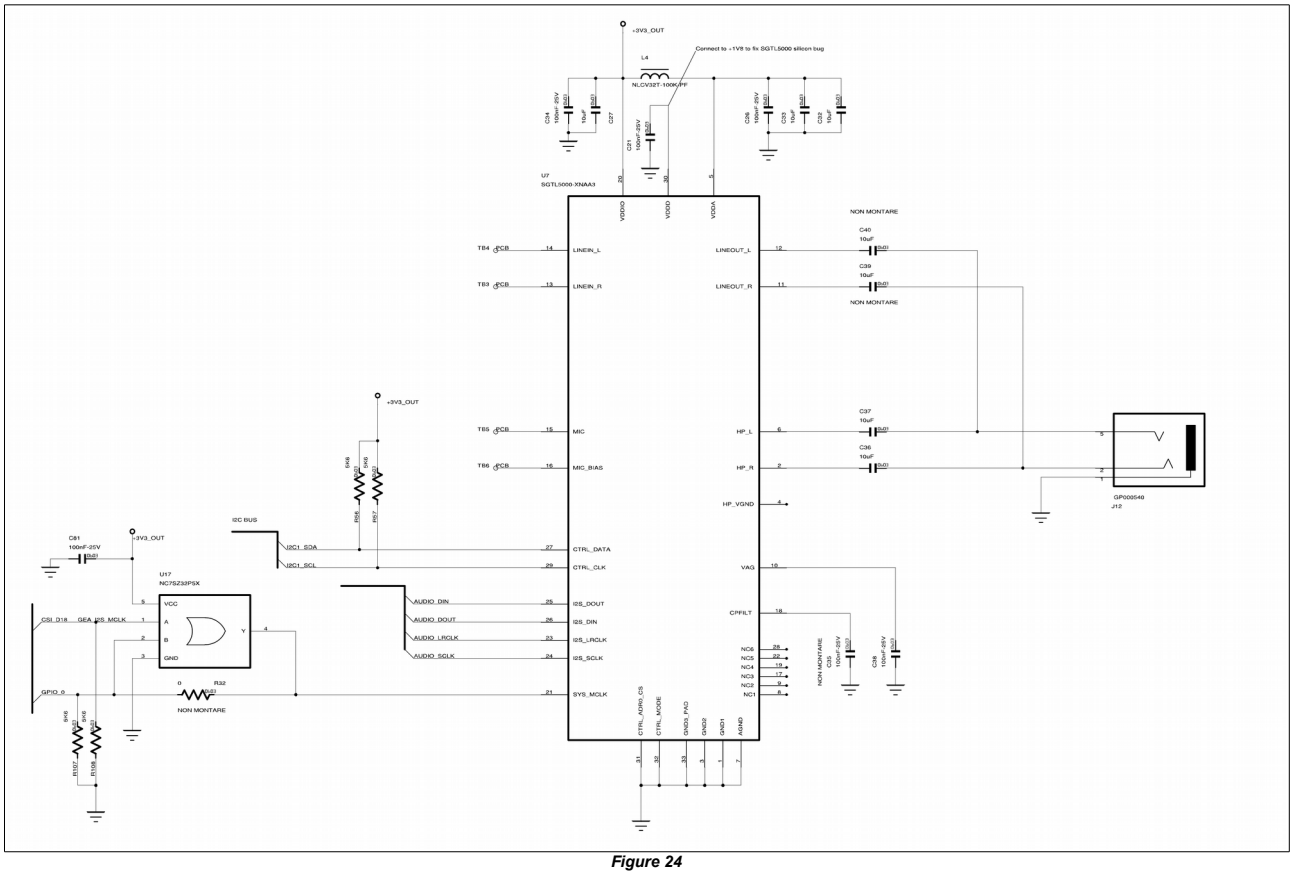

Figure 24

Following the I2S BUS pins numbering

Number	Name	Primary Function Description	GPIO Capable	Voltage
114	I2S_DIN	I2S Data In	Y	+3,3V
122	I2S_DOUT	I2S_Data OUT	Y	+3,3V
124	I2S_SCLK	I2S_SCLK	Y	+3,3V
115	I2S_LRCLK	I2S_LRCLK	Y	+3,3V

Table 25

WARNING!
To implement the SGTL5000 on the carrier board, remember to connect the VDD, pin 30 of the SGTL5000 device, to +1V8 to fix a silicon bug (for further detail refer to SGTL5000 data sheet)

5.12 How to connect the reset pin

The nRESET signal has input/output functionality and shall be driven in open-drain mode. *The signal has an internal 100K pull-up and a 100 Ohm series resistors,the maximum recommended capacitive load is about* ***100pF.***

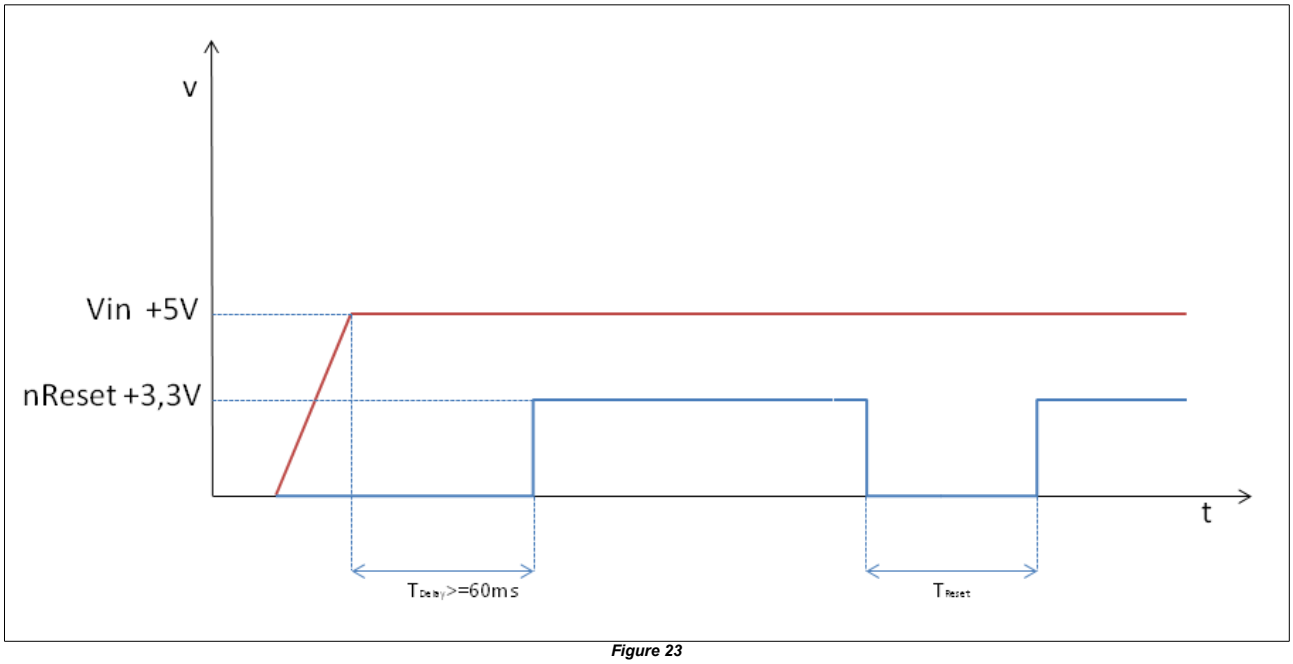

Figure 23

T_{Delay}: driven low by SOM during the POR state
T_{Reset}: driven low by user to force POR CPU pin

5.12.1 Input mode usage

The nRESET signal can be used to reset the module by driving it with an **open-drain** or with a simple button. If there are no special requirements, the module is fully auto-sufficient in terms of reset sequence, so its nRESET signal can be left floating. No Pull-up resistor is required on the carrier board; if a different pull-up resistor value (from the 100K on board of the module) is necessary, an additional pull-up on the carrier can be placed with values greater than 10K Ohm.

5.12.2 Output mode usage

The nRESET signal can also be used to monitor POR phase of the module, or to apply the reset (POR only) to other devices on the carrier. In this case, please take care to always respect limits imposed by maximum capacitive load and minimum additional pull-up.

WARNING: nReset is a POR signal only, therefore it may not be driven by the SOM during another CPU reset event (e.g. WDOG reset).

Chapter

6

6. Peripheral multiplexing

This Chapter gives the alternative peripheral informations

Section includes :

- ✔ **I2S**
- ✔ **SPI**
- ✔ **PWM**
- ✔ **GPT**
- ✔ **I2C**
- ✔ **UART**
- ✔ **CSI**
- ✔ **SD**

6.1 Peripheral multiplexing description

Following we describe opportunity to use alternative interfaces using the properties of multiplexing pin.
Please refer to the NXP's reference manual and documentation for further details (document name i.MX6UL Reference Manual).

6.1.1 SPI Interfaces

Using pin multiplexing 's features we may have the following SPI and IIS connections. In the tables below are shown the output signals on the Connector's module.

ECSPI1 signals interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
63 / 65	CSI_DATA06 / LCD_DATA22	MOSI	+3,3V
73 / 106	CSI_DATA07 / LCD_DATA23	MISO	+3,3V
72 / 108	CSI_DATA04 / LCD_DATA20	SCK	+3,3V
68 / 109	CSI_DATA05 / LCD_DATA21	SS0	+3,3V
153	LCD_DATA05	SS1	+3,3V
152	LCD_DATA06	SS2	+3,3V
151	LCD_DATA07	SS3	+3,3V

Table 26

ECSPI2 signals interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
170 / 111	CSI_DATA02 / UART5_TX_DATA	MOSI	+3,3V
166 / 110	CSI_DATA03 / UART5_RX_DATA	MISO	+3,3V
168 / 23	CSI_DATA00 / UART4_TX_DATA	SCK	+3,3V
171 / 24	CSI_DATA01 / UART4_RX_DATA	SS0	+3,3V
161	LCD_HSYNC	SS1	+3,3V
160	LCD_VSYNC	SS2	+3,3V
62	LCD_RESET	SS3	+3,3V

Table 27

ECSPI3 signals interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
35	NAND_CE1_B / UART2_CTS_B	MOSI	+3,3V
121	UART2_RTS_B	MISO	+3,3V
113	UART2_RX_DATA	SCK	+3,3V
112	UART2_TX_DATA	SS0	+3,3V

Table 28

6.1.2 IIS Configuration

The following tables show the pin configurations for IIS Bus on module's connector.

IIS1 bus interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
63 / 155	CSI_DATA06 / LCD_DATA03	I2S_DIN	+3,3V
73 / 154	CSI_DATA07 / LCD_DATA04	I2S_DOUT	+3,3V
68 / 157	CSI_DATA05 / LCD_DATA02	I2S_SCLK	+3,3V
171 / 159	CSI_DATA01 / LCD_DATA00	I2S_MCLK	+3,3V
72 / 158	CSI_DATA04 / LCD_DATA01	I2S_LRCLK	+3,3V

Table 29

IIS2 bus interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
114 / 185	JTAG_TCK / SD1_DATA2	I2S_DIN	+3,3V
122 / 186	JTAG_TRST_B / SD1_DATA3	I2S_DOUT	+3,3V
124 / 187	JTAG_TDI / SD1_DATA1	I2S_SCLK	+3,3V
34 / 189	JTAG_TMS / SD1_CLK	I2S_MCLK	+3,3V
115 / 188	JTAG_TDO / SD1_DATA0	I2S_LRCLK	+3,3V

Table 30

IIS3 bus interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
144	LCD_DATA14	I2S_DIN	+3,3V
143 / 62	LCD_DATA15 / LCD_RESET	I2S_DOUT	+3,3V
147	LCD_DATA11	I2S_SCLK	+3,3V
125 / 149	LCD_CLK / LCD_DATA09	I2S_MCLK	+3,3V
146 / 162	LCD_DATA12 / LCD_ENABLE	I2S_LRCLK	+3,3V

Table 31

6.1.3 Alternative PWM pins table

It's possible to set the pins shown in the following table as PWM signals.

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
38 / 159	GPIO1_IO08 / LCD_DATA00	PWM-1	+3,3V
184 /158	GPIO1_IO09 / LCD_DATA01	PWM-2	+3,3V
25 / 157	GPIO1_IO04 / LCD_DATA02	PWM-3	+3,3V
155	LCD_DATA03	PWM-4	+3,3V
15 / 36	LCD_DATA18 / NAND_DQS	PWM-5	+3,3V
124 / 16	JTAG_TDI / LCD_DATA19	PWM-6	+3,3V
169 / / 114	CSI_VSYNC / JTAG_TCK	PWM-7	+3,3V
167 / 132 / 122	CSI_HSYNC / ENET1_RX_ER / JTAG_TRST_B	PWM-8	+3,3V

Table 32

6.1.4 General Purpose Timer (GPT)

Using pin multiplexing 's features we may have the following GPT connections. In the tables below are shown the signals on the Connector's module.

GPT IN interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
33 / 112	GPIO1_IO00 / UART2_TX_DATA	GPT 1 - CAPIN1	+3,3V
113 / 132	UART2_RX_DATA / ENET1_RX_ER	GPT 1 - CAPIN2	+3,3V
185	SD1_DATA2	GPT 2 - CAPIN1	+3,3V
186	SD1_DATA3	GPT 2 - CAPIN2	+3,3V

Table 33

GPT OUT interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
28 / 116	GPIO1_IO01 / UART1_TX_DATA	GPT1_CMPOUT1	+3,3V
27 / 120	GPIO1_IO02 / UART2_CTS_B	GPT1_CMPOUT2	+3,3V
27 / 121	UART2_RTS_B	GPT1_CMPOUT3	+3,3V
19	SD1_CMD	GPT2_CMPOUT1	+3,3V
189	SD1_CLK	GPT2_CMPOUT2	+3,3V
188	SD1_DATA0	GPT2_CMPOUT3	+3,3V

Table 34

GPT CLK interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
117	UART1_RX_DATA	GPT1_CLKIN	+3,3V
187	SD1_DATA1	GPT2_CLKIN	+3,3V

Table 35

6.1.5 I2C Configuration

The following tables show the pin configurations for I2C Bus on module's connector.

I2C1 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
40 / 27 / 23	CSI_PIXCLK / GPIO1_IO02 / UART4_TX_DATA	SCL	+3,3V
37 / 26 / 24	CSI_MCLK / GPIO1_IO03 / UART4_RX_DATA	SDA	+3,3V

Table 36

I2C2 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
167 / 33 / 111	CSI_HSYNC / GPIO1_IO00 / UART5_TX_DATA	SCL	+3,3V
169 / 28 / 110	CSI_VSYNC / GPIO1_IO01 / UART5_RX_DATA	SDA	+3,3V

Table 37

I2C3 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
158 / 116	LCD_DATA01 / UART1_TX_DATA	SCL	+3,3V
159 / 117	LCD_DATA00 / UART1_RX_DATA	SDA	+3,3V

Table 38

I2C4 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
155 / 112	LCD_DATA03 / UART2_TX_DATA	SCL	+3,3V
157 / 113	LCD_DATA02 / UART2_RX_DATA	SDA	+3,3V

Table 39

6.1.6 Alternative UART pins tables

The following tables shows an alternative UART configuration

UART1 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
79	UART1_CTS_B	UART1_CTS	+3,3V
183	UART1_RTS_B	UART1_RTS	+3,3V
27 / 116	GPIO1_IO02 / UART1_TX_DATA	UART1_TXD	+3,3V
26 / 117	GPIO1_IO03 / UART1_RX_DATA	UART1_RXD	+3,3V

Table 40

UART2 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
120	UART2_CTS_B	UART2_CTS	+3,3V
66 / 121	UART3_RX_DATA / UART2_RTS_B	UART2_RTS	+3,3V
112	UART2_TX_DATA	UART2_TXD	+3,3V
113	UART2_RX_DATA	UART2_RXD	+3,3V

Table 41

UART3 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
35 / 118	NAND_CE1_B / UART3_CTS_B	UART3_CTS	+3,3V
119	UART3_RTS_B	UART3_RTS	+3,3V
191	UART3_TX_DATA	UART3_TXD	+3,3V
66	UART3_RX_DATA	UART3_RXD	+3,3V

Table 42

UART4 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
161	LCD_HSYNC	UART4_CTS	+3,3V
160	LCD_VSYNC	UART4_RTS	+3,3V
125 / 23	LCD_CLK / UART4_TX_DATA	UART4_TXD	+3,3V
162 / 24	LCD_ENABLE / UART4_RX_DATA	UART4_RXD	+3,3V

Table 43

UART5 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
166 / 184	CSI_DATA03 / GPIO1_IO09	UART5_CTS	+3,3V
170 / 38	CSI_DATA02 / GPIO1_IO08	UART5_RTS	+3,3V
168 / 25 / 111	CSI_DATA00 / GPIO1_IO04 / UART5_TX_DATA	UART5_TXD	+3,3V
171 / 110	CSI_DATA01 / UART5_RX_DATA	UART5_RXD	+3,3V

Table 44

UART6 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
167	CSI_HSYNC	UART6_CTS	+3,3V
169	CSI_VSYNC	UART6_RTS	+3,3V
37	CSI_MCLK	UART6_TXD	+3,3V
40	CSI_PIXCLK	UART6_RXD	+3,3V

Table 45

UART7 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
152	LCD_DATA06	UART7_CTS	+3,3V
132 / 151	ENET1_RX_ER / LCD_DATA07	UART7_RTS	+3,3V
142	LCD_DATA16	UART7_TXD	+3,3V
141	LCD_DATA17	UART7_RXD	+3,3V

Table 46

UART8 interfaces

Pin number	Pin Name on i.MX	Signal reference	Voltage reference
105 / 154	ENET2_TX_CLK / LCD_DATA04	UART8_CTS	+3,3V
106 / 153	LCD_DATA23 / LCD_DATA05	UART8_RTS	+3,3V
108	LCD_DATA20	UART8_TXD	+3,3V
109	LCD_DATA21	UART8_RXD	+3,3V

Table 47

6.1.7 Alternative CMOS Sensor Interface

CSI interfaces

Pin Number	Pin Name on i.MX	Signal Name	Function Description	Voltage
141 / 66	LCD_DATA17 / UART3_RX_DATA	DATA0	CMOS Sensor Interface Data	+3,3V
142 / 191	LCD_DATA16 / UART3_TX_DATA	DATA1	CMOS Sensor Interface Data	+3,3V
168 / 116	CSI_DATA00 / UART1_TX_DATA	DATA2	CMOS Sensor Interface Data	+3,3V
171 / 117	CSI_DATA01 / UART1_RX_DATA	DATA3	CMOS Sensor Interface Data	+3,3V
170 / 79	CSI_DATA02 / UART1_CTS_B	DATA4	CMOS Sensor Interface Data	+3,3V
166 / 183	CSI_DATA03 / UART1_RTS_B	DATA5	CMOS Sensor Interface Data	+3,3V
72 / 112	CSI_DATA04 / UART2_TX_DATA	DATA6	CMOS Sensor Interface Data	+3,3V
68 / 113	CSI_DATA05 / UART2_RX_DATA	DATA7	CMOS Sensor Interface Data	+3,3V
63 / 120	CSI_DATA06 / UART2_CTS_B	DATA8	CMOS Sensor Interface Data	+3,3V
73 / 121	CSI_DATA07 / UART2_RTS_B	DATA9	CMOS Sensor Interface Data	+3,3V
15 / 118	LCD_DATA18 / UART3_CTS_B	DATA10	CMOS Sensor Interface Data	+3,3V
16 / 119	LCD_DATA19 / UART3_RTS_B	DATA11	CMOS Sensor Interface Data	+3,3V
108 / 23	LCD_DATA20 / UART4_TX_DATA	DATA12	CMOS Sensor Interface Data	+3,3V
109 / 24	LCD_DATA21 / UART4_RX_DATA	DATA13	CMOS Sensor Interface Data	+3,3V
65 / 111	LCD_DATA22 / UART5_TX_DATA	DATA14	CMOS Sensor Interface Data	+3,3V
106 / 110	LCD_DATA23 / UART5_RX_DATA	DATA15	CMOS Sensor Interface Data	+3,3V
150	LCD_DATA08	DATA16	CMOS Sensor Interface Data	+3,3V
149	LCD_DATA09	DATA17	CMOS Sensor Interface Data	+3,3V
148	LCD_DATA10	DATA18	CMOS Sensor Interface Data	+3,3V
147	LCD_DATA11	DATA19	CMOS Sensor Interface Data	+3,3V
146	LCD_DATA12	DATA20	CMOS Sensor Interface Data	+3,3V
145	LCD_DATA13	DATA21	CMOS Sensor Interface Data	+3,3V
144	LCD_DATA14	DATA22	CMOS Sensor Interface Data	+3,3V
132 / 143	ENET1_RX_ER / LCD_DATA15	DATA23	CMOS Sensor Interface Data	+3,3V
36	NAND_DQS	FIELD	CMOS Sensor Interface Field Signal	+3,3V
167 / 184	CSI_HSYNC / GPIO1_IO09	MCLK	CMOS Sensor Interface Master CLK	+3,3V
37	CSI_MCLK	VSYNC	CMOS Sensor Interface Vertical Sync	+3,3V
40	CSI_PIXCLK	HSYNC	CMOS Sensor Interface Horizontal Sync	+3,3V
169 / 38	CSI_VSYNC / GPIO1_IO08	PIXCLK	CMOS Sensor Interface Pixel Clock	+3,3V

Table 48

6.1.8 uSDHC Interfaces

uSDHC Interface (SD1)

Pin Number	Pin Name on i.MX	Signal reference	Voltage reference
26 / 68 / 183	GPIO1_IO03 / CSI_DATA05 / UART1_RTS_B	uSDHC1 CD Signal	+3,3V
188	SD1_DAT0	uSDHC1 DAT 0 signal	+3,3V
187	SD1_DAT1	uSDHC1 DAT 1 signal	+3,3V
185	SD1_DAT2	uSDHC1 DAT 2 signal	+3,3V
186	SD1_DAT3	uSDHC1 DAT 3 signal	+3,3V
189	SD1_CLK	uSDHC1 CLK signal	+3,3V
190	SD1_CMD	uSDHC1 CMD signal	+3,3V

Table 49

uSDHC Interface (SD2) [1)]

Pin Number	Pin Name on i.MX	Signal reference	Voltage reference
37 / 183	CSI_MCLK / UART1_RTS_B	uSDHC2 CD Signal	+3,3V
108 / 168	LCD_DATA20 / CSI_DATA00	uSDHC2 DAT 0 signal	+3,3V
109 / 171	LCD_DATA21 / CSI_DATA01	uSDHC2 DAT 1 signal	+3,3V
65 / 170	LCD_DATA22 / CSI_DATA02	uSDHC2 DAT 2 signal	+3,3V
106 / 166	LCD_DATA23 / CSI_DATA03	uSDHC2 DAT 3 signal	+3,3V
16 / 169	LCD_DATA19 / CSI_VSYNC	uSDHC2 CLK signal	+3,3V
15 / 167	LCD_DATA18 / CSI_HSYNC	uSDHC2 CMD signal	+3,3V

Table 50

[1)] ***For the module equipped with eMMC the SD2 interface is not available***. *In this configuration, the pins in the table above, are always available for all the other alternative functions selectable by the processor's IOMUX,* ***except the SD2 peripheral*** *that is used for the manage of the eMMC interface.*