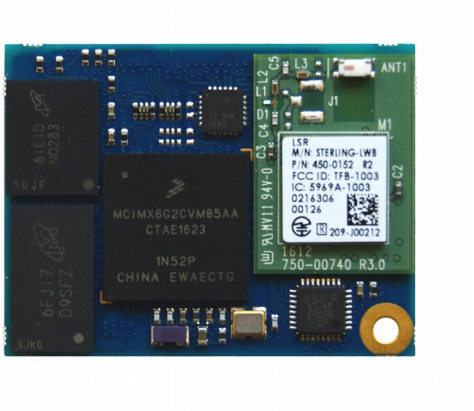
Is.IoT HW manual 1.0.3
Getting started manual



***** REV 1.0.3 *****

DATE	REVISION	CHANGE DESCRIPTION
14/12/2016	1.0.0	Release
09/01/2017	1.0.1	General enhancement
26/01/2017	1.0.2	Correction on UART MUX pad reference
14/02/2017	1.0.3	Added Mechanical insertion positioning and fixing. Added board adapter specifications

Summary

Chapter

1

1. Introduction

This Chapter gives background information on this document.

Section includes

- ✔ **General Overview**
- ✔ **Acronyms and Abbreviations Used**
- ✔ **Document and Standard References**

1.1 Introduction

This document is created to guide users to design IS.IOT MX6UL compliant carrier board. It will focus only on the interfaces in IS.IOT MX6UL pinouts and related peripherals.

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

All examples of this document are based on IS.IOT MX6UL carrier board that is available from ENGICAM. This document also provides a collection of useful documentation, application reports, and design recommendations.

1.2 Acronyms and Abbreviations used

ABBREVIATION	EXPLANATION
ADC	Analogue to Digital Converter
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CPU	Central Processor Unit
DAC	Digital to Analogue Converter
EMI	Electromagnetic Interference, high frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic- sensitive devices
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
HDMI	High-Definition Multimedia Interface, combines audio and video signal
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, colour channels in common display interfaces
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
USB	Universal Serial Bus, serial interface for internal and external peripherals

1.3 Document and Standard References

1.3.1 External Industry Standard Documents

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- USB Specifications (www.usb.org).

1.3.2 NXP Documents

- IMX6ULRM
- IMX6ULCEC
- USR_Guide
- AN5170
- AN5198
- IMX6ULHDG
- MX6ULEVKHDG
- IMX6ULCE
- IMX6ULTRALITEFS
- IMX6SRSFS

1.3.3 Disclaimer

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Chapter

2

2. Mechanical data

This Chapter gives information about PCB and module's dimensions.

Section includes

- ✔ **Assembly Top**
- ✔ **Assembly Bottom**
- ✔ **Mechanical dimensions**

2.1 Mechanical data

The i.MX6UL module has an interface compliant with Hirose code DF40C-90DS-0.4V or compatible connector. The PCB dimensions is L 40 x W 30 x H 1,2 mm. The distances under PCB for ICs component:

- using DF40C-90DS-0.4V(51) is not recommended the component positioning under the module
- using DF40HC(3.0)-90DS-0.4V(51) about 1,4 mm height available
- using DF40HC(4.0)-90DS-0.4V(51) about 2,4 mm height available

2.2 Assembly Top View

In the Figure below is shown top view assembly plan.

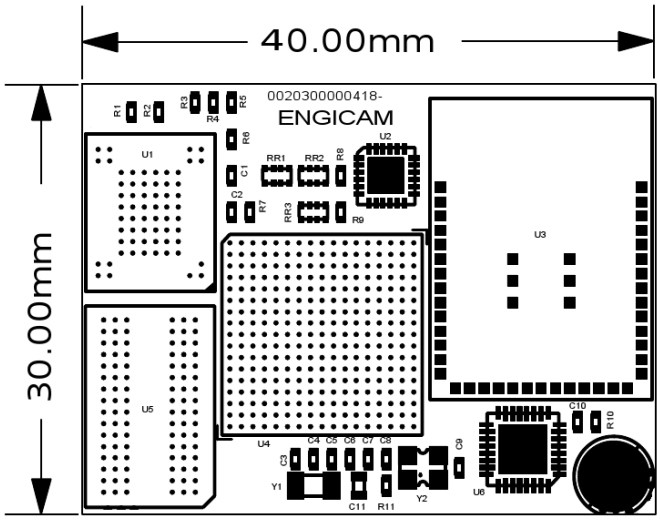


Figure 1

2.3 Assembly Bottom View

In the Figure below is shown bottom view assembly plan.

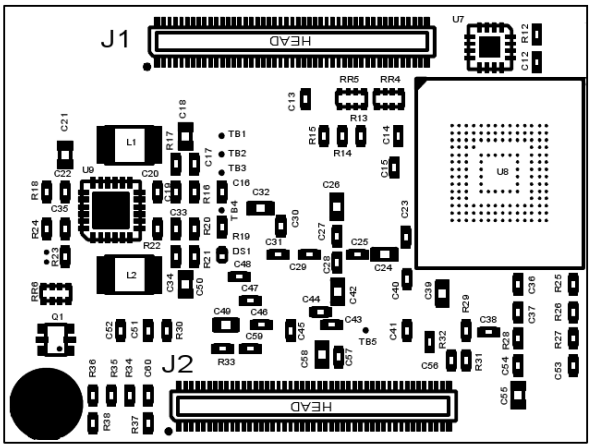


Figure 2

Chapter

3

3. Ordering Information and Features

This Chapter gives the ordering information and technical specifications of the modules.

Section includes

- ✔ **IS.IOT MX6UL Ordering code**
- ✔ **CPU & memory specifications**
- ✔ **Operating temperature range**

3.1 Ordering Information

Following we provide the ordering informations and the description for the Basic technical specifications modules:

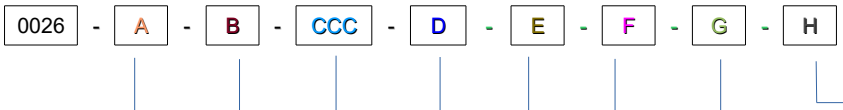
Part name	Ordering Code	MPQ	Description	CPU & Memory specifications	CPU junction temperature range °C	Operating temperature range °C (excepted CPU)	Module available at least until [1]
Is.IoT MX6UL	**00268W0052E410**	1	Is.IoT MX6UL eMMC Wireless	i.MX6UL, MCIMX6G2, 528MHz,128MB DDR3, 4GB eMMC, WiFi+BT, Single Ethernet, Ext temp consumer	-40 to +105	-20 to +85 [2]	4 th Q - 2030
Is.IoT MX6UL	**00267W0052E410**	58	Is.IoT MX6UL eMMC Wireless		-40 to +105	-20 to +85 [2]	4 th Q - 2030
Is.IoT MX6UL	**00268W0052I010**	1	Is.IoT MX6UL NAND Wireless	i.MX6UL MCIMX6G2, 528MHz,128MB DDR3, 256MB NAND, WiFi+BT, Single Ethernet, Industrial	-40 to +105	-40 to +85	4 th Q - 2030
Is.IoT MX6UL	**00267W0052I010**	58	Is.IoT MX6UL NAND Wireless		-40 to +105	-40 to +85	4 th Q - 2030
Is.IoT MX6UL	**0026800052I010**	1	Is.IoT MX6UL NAND Wired	i.MX6UL MCIMX6G2, 528MHz,128MB DDR3, 256MB NAND, Single Ethernet, Industrial	-40 to +105	-40 to +85	4 th Q - 2030
Is.IoT MX6UL	**0026700052I010**	58	Is.IoT MX6UL NAND Wired		-40 to +105	-40 to +85	4 th Q - 2030

Table 1

[1] **Long Term Availability based on NXP longevity program**

[2] **Consumer eMMC with extended temperature**

The module is available with both option NAND or eMMC. It's also possible to order the module with Wi-Fi and Bluetooth. *The standard order codes shown in the tables above shall be modified as follow:*



H	Reserved

MPQ	A
58	7
1	8

G	RAM SIZE
0	64MB
1	128MB
2	256MB
3	512MB
-	-
-	-

OPTION AVAILABLE	B
No option	0
WiFi + BT Sterling mounted	W
-	-

F	SPECIFICATIONNON VOLATILE MEMORY
0	256MB SLC NAND
-	-
-	-
4	4GB eMMC
-	-

SOM TYPE	CCC
Is.IoT MX6UL	005
-	-
-	-
-	-
-	-

E	TEMPERATURE QUALIFIER
-	-
E	Extended Temperature
I	Industrial
-	-

CPU TYPE RELATED TO SOM	D
-	-
-	-
G2	2
-	-

Ordering Code nomenclature

Chapter

4

4. Pinout

This Chapter gives the pinout informations.

Section includes

- ✔ **Pinout overview**
- ✔ **i.MX Pad spacifications**
- ✔ **Electrical specification**

4.1 Module Pinout

The module's interface is achieved by 2 connector HIROSE code DF40C-90DP or compatible

A -CONNECTOR

ODD	NAME	PAD on i.MX	DESCRIPTION	EVEN	NAME	PAD on i.MX	DESCRIPTION
1	+VIN	-	Main voltage input	2	+VIN	-	Main voltage input
3	+VIN	-	Main voltage input	4	+VIN	-	Main voltage input
5	+VIN	-	Main voltage input	6	+VIN	-	Main voltage input
7	+VIN	-	Main voltage input	8	+VIN	-	Main voltage input
9	DNC	-	Do Not Connect	10	DNC	-	Do Not Connect
11	USB0_VBUS	USB_OTG1_VBUS	+5V USB VBUS	12	+3,3V	-	Output Power PIN
13	USB0_DP	USB_OTG1_DP	USB0 2.0 TXRX lane	14	+3,3V	-	Output Power PIN
15	USB0_DM	USB_OTG1_DM	USB0 2.0 TXRX lane	16	GND	-	Ground
17	USB0_ID	USB_OTG1_ID	USB0 OTG ID signal	18	I2C0_SDA	UART4_RX_DATA	I2C data (pull-up needed on carrier)
19	LCD_BKL_PWM	ENET1_RX_ER	LCD backlight PWM	20	I2C0_SCL	UART4_TX_DATA	I2C data (pull-up needed on carrier)
21	GPIO_0	UART1_CTS	GENERAL GPIO	22	+3,3V	-	Output Power PIN
23	GPIO_1	UART3_DX_DATA	GENERAL GPIO	24	+3,3V	-	Output Power PIN
25	GPIO_2	LCD_RESET	GENERAL GPIO	26	SD1_DET [3)]	UART_RTS	SDIO CARD Detect
27	*GPIO_3*	NAND_CE1	GENERAL GPIO	28	SD1_DAT0 [3)]	SD1_DATA0	SDIO data 0
29	*GPIO_4*	SNVS_TAMPER0	GENERAL GPIO	30	SD1_DAT1 [3)]	SD1_DATA1	SDIO data 1
31	GPIO_5	SNVS_TAMPER1	GENERAL GPIO	32	SD1_DAT2 [3)]	SD1_DATA2	SDIO data 2
33	*GPIO_6*	SNVS_TAMPER2	GENERAL GPIO	34	SD1_DAT3 [3)]	SD1_DATA3	SDIO data 3
35	I2S_CLK	JTAG_TDI	AUDIO I2S clk	36	GND	-	Ground
37	I2S_IN	JTAG_TCK	AUDIO I2S input	38	SD1_CLK [3)]	SD1_CLK	SDIO clock

ODD	NAME	PAD on i.MX	DESCRIPTION	EVEN	NAME	PAD on i.MX	DESCRIPTION
39	I2S_OUT	JTAG_TRST	AUDIO I2S output	40	SD1_CMD 3)	SD1_CMD	SDIO cmd
41	I2S_FRM	JTAG_TDO	AUDIO I2S frame	42	GND	-	Ground
43	GND	-	Ground	44	SPI0_SS0	ENET2_RX_ER	SPI Slave select
45	I2S_MCLK	JTAG_TMS	AUDIO I2S master clock	46	SPI0_CLK	ENET2_TX_DATA1	SPI clock
47	GND	-	Ground	48	SPI0_MOSI	ENET2_TX_EN	SPI MOSI
49	UART0_TX	UART2_TX_DATA	UART TX OUT	50	SPI0_MISO	ENET2_TX_CLK	SPI MISO
51	UART0_RX	UART2_RX_DATA	UART RX IN	52	GND	-	Ground
53	UART0_RTS	UART2_CTS	UART RTS OUT	54	CONUART_TX	UART1_TX_DATA	OS Console
55	UART0_CTS	UART2_RTS	UART CTS IN	56	CONUART_RX	UART1_RX_DATA	OS Console
57	UART1_TX	UART8_TX_DATA	UART TX OUT	58	BOOT_SEL0	BOOT_MODE1	Recovery boot
59	UART1_RX	UART8_RX_DATA	UART RX IN	60	BOOT_SEL1	-	Alternative boot (SD card)
61	GND	-	Ground	62	NC	-	Not Connect
63	+VCOIN 2)	VDD_SNVS_IN	CPU RTC backup voltage	64	#RESET	POR	Module reset input (drive it with open drain)
65	DNC	-	Do Not Connect	66	PWM0	NAND_DQS	PWM output
67	GND	-	Ground	68	GND	-	Ground
69	LCD_D00	LCD_DATA00	LCD parallel signal	70	LCD_D11	LCD_DATA11	LCD parallel signal
71	LCD_D01 1)	LCD_DATA01	LCD parallel signal	72	LCD_D12 1)	LCD_DATA12	LCD parallel signal
73	LCD_D02 1)	LCD_DATA02	LCD parallel signal	74	LCD_D13 1)	LCD_DATA13	LCD parallel signal
75	LCD_D03 1)	LCD_DATA03	LCD parallel signal	76	LCD_D14 1)	LCD_DATA14	LCD parallel signal
77	LCD_D04 1)	LCD_DATA04	LCD parallel signal	78	LCD_D15 1)	LCD_DATA15	LCD parallel signal
79	LCD_D05 1)	LCD_DATA05	LCD parallel signal	80	LCD_D16 1)	LCD_DATA16	LCD parallel signal
81	LCD_D06 1)	LCD_DATA06	LCD parallel signal	82	LCD_D17 1)	LCD_DATA17	LCD parallel signal
83	LCD_D07 1)	LCD_DATA07	LCD parallel signal	84	LCD_OE	LCD_ENABLE	LCD parallel signal
85	LCD_D08 1)	LCD_DATA08	LCD parallel signal	86	LCD_HSYNC	LCD_HSYNC	LCD parallel signal

ODD	NAME	PAD on i.MX	DESCRIPTION		EVEN	NAME	PAD on i.MX	DESCRIPTION
87	LCD_D09 [1)]	LCD_DATA09	LCD parallel signal		88	LCD_VSYNC	LCD_VSYNC	LCD parallel signal
89	LCD_D10 [1)]	LCD_DATA10	LCD parallel signal		90	LCD_CLK	LCD_CLK	LCD parallel signal

Table 2

B -CONNECTOR

ODD	NAME	PAD on i.MX	DESCRIPTION		EVEN	NAME	PAD on i.MX	DESCRIPTION
1	NC	-	Not Connect		2	USB1_VBUS	USB_OTG2_VBUS	+5V USB VBUS
3	NC	-	Not Connect		4	USB1_DP	USB_OTG2_DP	USB0 2.0 TXRX lane
5	GND	-	Ground		6	USB1_DM	USB_OTG2_DN	USB0 2.0 TXRX lane
7	NC	-	Not Connect		8	NC	-	Not Connect
9	NC	-	Not Connect		10	NC	-	Not Connect
11	GND	-	Ground		12	NC	-	Not Connect
13	NC	-	Not Connect		14	GND	-	Ground
15	NC	-	Not Connect		16	NC	-	Not Connect
17	GND	-	Ground		18	NC	-	Not Connect
19	NC	-	Not Connect		20	GND	-	Ground
21	NC	-	Not Connect		22	NC	-	Not Connect
23	GND	-	Ground		24	NC	-	Not Connect
25	NC	-	Not Connect		26	GND	-	Ground
27	NC	-	Not Connect		28	I2C1_SDA	GPIO1_IO01	I2C clock (pull-up needed on carrier)
29	GND	-	Ground		30	I2C1_SCL	GPIO1_IO00	I2C clock (pull-up needed on carrier)
31	ETH_MDI0+	-	ETH Gb lane 0 or 10/100 Tx		32	NC	-	Not Connect
33	ETH_MDI0-	-	ETH Gb lane 0 or 10/100 Tx		34	NC	-	Not Connect
35	ETH_CTREF	-	Mid point reference		36	GND	-	Ground

ODD	NAME	PAD on i.MX	DESCRIPTION	EVEN	NAME	PAD on i.MX	DESCRIPTION
37	ETH_MDI1+	-	ETH Gb lane 1 or 10/100 Rx	38	NC	-	Not Connect
39	ETH_MDI1-	-	ETH Gb lane 1 or 10/100 Rx	40	NC	-	Not Connect
41	ETH_LINK#	-	Link led driver	42	ETH_ACT#	-	Activity led driver
43	NC	-	Not Connect	44	NC	-	Not Connect
45	NC	-	Not Connect	46	NC	-	Not Connect
47	GND	-	Ground	48	GND	-	Ground
49	NC	-	Not Connect	50	NC	-	Not Connect
51	NC	-	Not Connect	52	NC	-	Not Connect
53	GND	-	Ground	54	GND	-	Ground
55	DNC	-	Do Not Connect	56	DNC	-	Do Not Connect
57	DNC	-	Do Not Connect	58	DNC	-	Do Not Connect
59	GND	-	Ground	60	GND	-	Ground
61	DNC	-	Do Not Connect	62	DNC	-	Do Not Connect
63	DNC	-	Do Not Connect	64	DNC	-	Do Not Connect
65	GND	-	Ground	66	GND	-	Ground
67	DNC	-	Do Not Connect	68	DNC	-	Do Not Connect
69	DNC	-	Do Not Connect	70	DNC	-	Do Not Connect
71	CSI_DATA00	CSI_DATA00	Camera CSI parallel signal	72	CSI_MCLK	CSI_MCLK	Camera CSI parallel signal
73	CSI_DATA01	CSI_DATA01	Camera CSI parallel signal	74	CSI_PIXCLK	CSI_PIXCLK	Camera CSI parallel signal
75	CSI_DATA02	CSI_DATA02	Camera CSI parallel signal	76	GPIO_IO01	GPIO1_IO02	General GPIO
77	CSI_DATA03	CSI_DATA03	Camera CSI parallel signal	78	GPIO_IO04	GPIO1_IO04	General GPIO
79	CSI_DATA04	CSI_DATA04	Camera CSI parallel signal	80	GPIO_IO05	GPIO1_IO05	General GPIO
81	CSI_DATA05	CSI_DATA05	Camera CSI parallel signal	82	GPIO_IO06	GPIO1_IO06	General GPIO
83	CSI_DATA06	CSI_DATA06	Camera CSI parallel signal	84	GPIO_IO07	GPIO1_IO07	General GPIO

ODD	NAME	PAD on i.MX	DESCRIPTION		EVEN	NAME	PAD on i.MX	DESCRIPTION
85	CSI_DATA07	CSI_DATA07	Camera CSI parallel signal		86	GPIO_IO10	JTAG_MOD	General GPIO
87	CSI_HSYNC	CSI_HSYNC	Camera CSI parallel signal		88	CAN1_TX	UART3_CTS	CAN TX
89	CSI_VSYNC	CSI_VSYNC	Camera CSI parallel signal		90	CAN1_RX	UART3_RTS	CAN RX

Table 3

The yellow lines highlight the required minimum electrical connections in order to make the module working correctly.

[1] *Note: for the use of this pin please refer to boot option in "**Boot Mode Pin"** chapter*

[2] *Connect to Coin-Cell or Super-Cap; left floating if not used*

[3] **Only for the module with Wi-Fi – BT option: the SD1 signals are shared between the SDIO pins of the A Connector and Wi-Fi interface. The SDIO pins are available only when nSD_BOOT signal is asserted. In this case the Wi-Fi interface is not available and SDIO signals become available for on module NAND/eMMC programming purpose**

4.2 Electrical specifications

	V Min (Volts)	V Typ (Volts)	V Max (Volts)
Vin [1)]	tbd	+ 5	+ 5,5
VBUS_OTG_USB, VBUS_USB	tbd	-	5.35
GPIO V(oh)	+ 3,15	-	-
GPIO V(ol)	-	-	+ 0,15
GPIO V(ih)	+ 2,35		+ 3,3
GPIO V(il)	0	-	+ 1

Table 4

[1)] This measure has done testing the module's start at the limit temperatures of -40°C and +85°C

Module	Test condition	Current @ 5V Min	Current @ 5V Typ	Current @ 5V Max
IS.IOT MX6UL NAND	Linux Sleep mode	-	20 mA	-
	Linux (only standard services running)	-	90 mA	110 mA
	QT, 2D dynamic graphic application running	-	150 mA	170 mA

Table 5

Module	Test condition	Current @ 5V Min	Current @ 5V Typ	Current @ 5V Max
IS.IOT MX6UL NAND Wi-Fi + Bluetooth	Linux Sleep mode	-	27 mA	-
	Linux (only standard services running)	-	100 mA	120 mA
	QT, 2D dynamic graphic application running	-	160 mA	180 mA

Table 6

Module	Test condition	Current @ 5V Min	Current @ 5V Typ	Current @ 5V Max
IS.IOT MX6UL eMMC	Linux Sleep mode	-	22 mA	-
	Linux (only standard services running)	-	90 mA	110 mA
	QT, 2D dynamic graphic application running	-	150 mA	190 mA

Table 7

Module	Test condition	Current @ 5V Min	Current @ 5V Typ	Current @ 5V Max
IS.IOT MX6UL eMMC Wi-Fi + Bluetooth	Linux Sleep mode	-	30 mA	-
	Linux (only standard services running)	-	100 mA	120 mA
	QT, 2D dynamic graphic application running	-	160 mA	200 mA

Table 8

Chapter

5

5. Carrier Board Design

This Chapter gives the technical specifications for carrier board design.

Section includes

- ✔ **Carrier Board recommendations**
- ✔ **Power signals and backup battery**
- ✔ **Serials**
- ✔ **CAN Bus**
- ✔ **Ethernet**
- ✔ **USB**
- ✔ **SDIO**
- ✔ **LCD**
- ✔ **Wi-Fi & Bluetooth**
- ✔ **Boot mode**
- ✔ **Audio**
- ✔ **Reset pin management**

5.1 Carrier board recommended specifications

5.1.1 Planarity in finish process

Due to the technical and mechanical specifications of the connector we suggest the maximum planarity of the footprint on PCB, so we suggest a type of finish obtained by horizontal process (we suggest and use for our carrier boards a type Chemical Gold finish).

5.1.2 Planarity of PCB

Also the planarity of the entire Printed Circuit Board must be kept in check especially when the your carrier board grows in size. In this case we suggest you contact the manufacturer of PCB to understand how improve the planarity of ended board and optimize the process maintaining the electrical characteristics unchanged

5.1.3 Power Supply

It's strongly recommended that the power supply of the carrier board, which feeds the driver and control devices connected with the i.MX processor, begins to work after the initialization of the processor itself

5.1.4 Module Positioning and fixing

Following, the mechanical positioning of the connectors on the carrier board used to insert the Is.IoT module

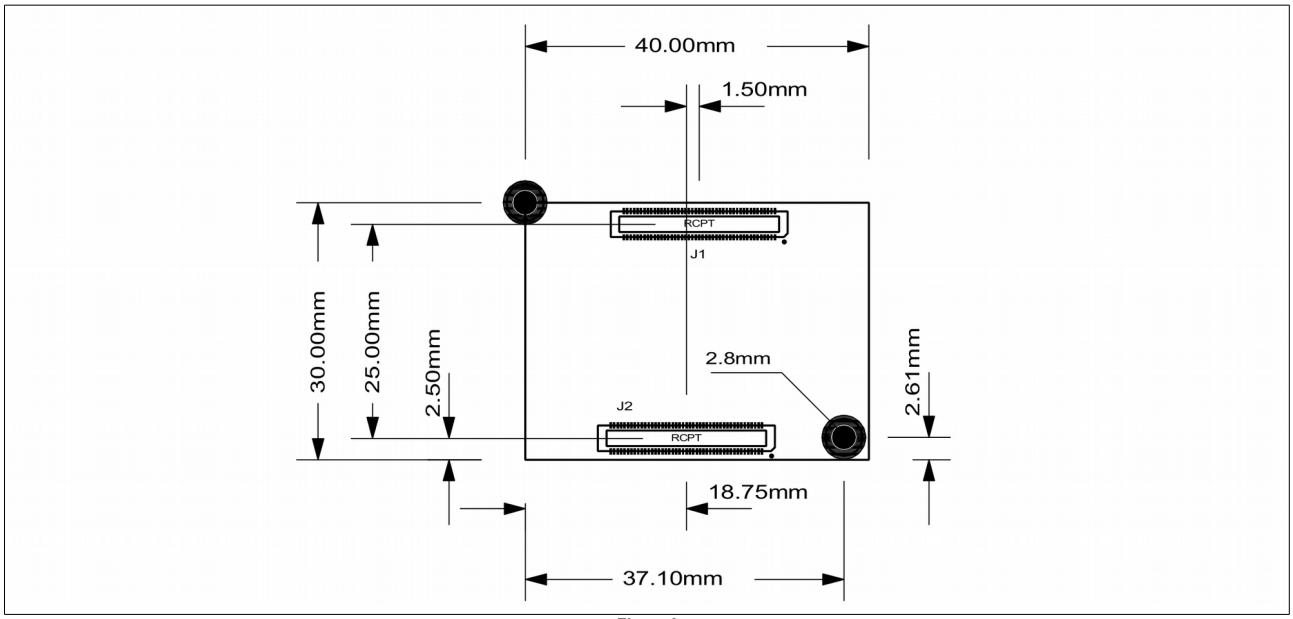


Figure 3

5.2 How to power the module

Please read carefully the related sections before start your power stage design. This module needs to be supply up to +5Vin power. Please refer to the table below for the power supply range specification. The power dissipated by the module in the operating mode is about 200 mA, but **the system must provide at least a power of 2A at 5V to allow the start of the module.**

In the following table are shown the module power supply pins numbering, please connect all power supply pins in order to avoid damage.

A connector	B connector	Name	Primary Function Description	GPIO Capable	Voltage
1	-	+5Vin	Power PIN	N	-
2	-	+5Vin	Power PIN	N	-
3	-	+5Vin	Power PIN	N	-
4	-	+5Vin	Power PIN	N	-
5	-	+5Vin	Power PIN	N	-
6	-	+5Vin	Power PIN	N	-
7	-	+5Vin	Power PIN	N	-
8	-	+5Vin	Power PIN	N	-
16	-	GND	Power PIN	N	-
36	-	GND	Power PIN	N	-
42	-	GND	Power PIN	N	-
43	-	GND	Power PIN	N	-
47	-	GND	Power PIN	N	-
52	-	GND	Power PIN	N	-
61	-	GND	Power PIN	N	-
67	-	GND	Power PIN	N	-
68	-	GND	Power PIN	N	-
-	5	GND	Power PIN	N	-
-	11	GND	Power PIN	N	-
-	14	GND	Power PIN	N	-
-	17	GND	Power PIN	N	-
-	20	GND	Power PIN	N	-
-	23	GND	Power PIN	N	-
-	26	GND	Power PIN	N	-
-	29	GND	Power PIN	N	-
-	36	GND	Power PIN	N	-
-	47	GND	Power PIN	N	-
-	48	GND	Power PIN	N	-
-	53	GND	Power PIN	N	-
-	54	GND	Power PIN	N	-

A connector	B connector	Name	Primary Function Description	GPIO Capable	Voltage
-	59	GND	Power PIN	N	-
-	60	GND	Power PIN	N	-
-	65	GND	Power PIN	N	-
-	66	GND	Power PIN	N	-

Table 9

In the following the pin used for voltage reference and for SD supply

A connector	B connector	Name	Primary Function Description	GPIO Capable	Voltage
12	-	VGPIO_REF [1)]	GPIO Power ref	N	+3,3V
14	-	VGPIO_REF [1)]	GPIO Power ref	N	+3,3V
22	-	SD1_VOUT [2)]	SD Supply Voltage	N	+3,3V
24	-	SD1_VOUT [2)]	SD Supply Voltage	N	+3,3V
-	35	ETH_CTREF [3)]	Mid Point reference	N	+3,3V

Table 10

[1)] In the following table are shown the maximum rating power for VGPIO_REF

Power output	Max output current
+3V3	300 mA (Total)

Table 11

[2)] These pins are used to SD Card supply voltage

[3)] Middle point reference for Ethernet interface (see chapter 5.6)

For further details on the power supply please refer to "i.MX 6UL" Data Sheet and Reference Manual.

5.2.1 How to connect a backup battery

The module allows the use of lithium rechargeable battery or supercapacitor as backup battery.
The connection with module is obtained by connecting directly the backup battery to the +Vcoin signal (pin 63 floating if not used).

The consumption of the pin is given by NXP for a maximum of 300uA
Note: *The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.*

Note: *The module is already designed to manage the charge of backup battery.*

For further details on the power supply please refer to "i.MX 6UL" Data Sheet and Reference Manual.

5.3 How to connect two 3-wire RS232 serial port

In this section is shown how to use the UART1 and UART2 as 3-wire RS232 serial ports.
In the following table are shown the UART1 and UART2 pins numbering.

A connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
57	UART1_TXD	UART TXD signal	LCD_DATA20	Y	+3,3V
59	UART1_RXD	UART RXD signal	LCD_DATA21	Y	+3,3V
54	CONUART_TXD *	OS Console	UART1_TX_DATA	Y	+3,3V
56	CONUART_RXD *	OS Console	UART1_RX_DATA	Y	+3,3V

Table 12

The signal on the module's UART pins are 3.3V logic level, this can not be connected directly to a RS232 device like a PC Serial port, the use of a transceivers on the base board is mandatory in order to avoid module damage.

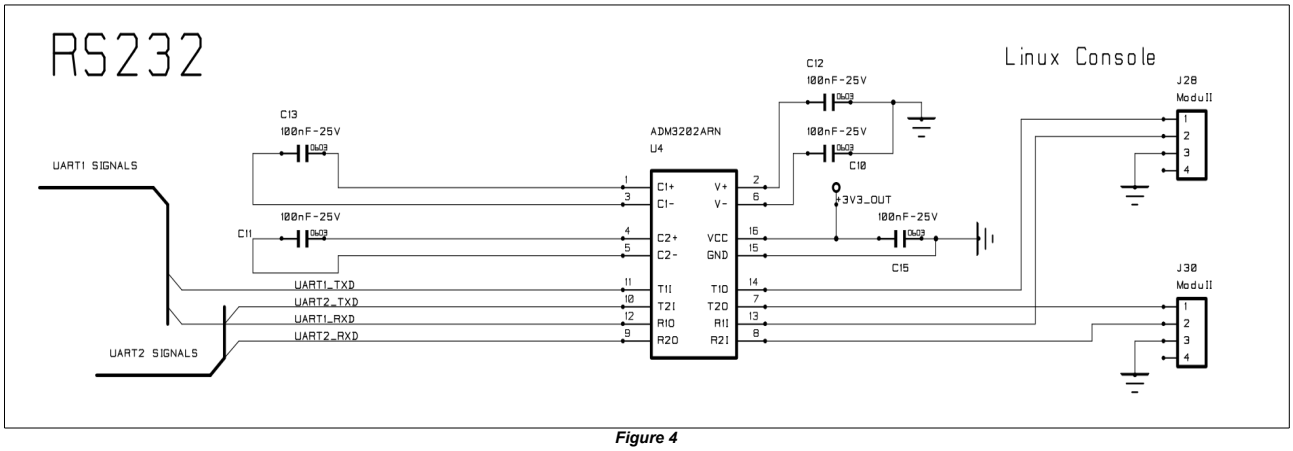


Figure 4

In this example an ADM3202ARN IC from Analog Device is used like transceiver for both UART without any control signal. In case RTS and CTS are need, a transceiver must be used for this signals.

When Linux is installed on a module, UART1 is used like console. The default communications settings is shown in the table below.

Linux console default settings	
Baud rate	115200
Data length	8 bit
Parity	none
Stop	1bit

Table 13

* **Note**: *the CONUART is used as Linux Console*

5.4 How to connect a RS485 serial port

In this chapter is shown how an RS485 serial port can be connected to the module. In the figure below is shown how UART3 is used to connect to a RS485 transceiver on the starter kit. The figure shows UART3 connection but you can consider that also UART 4 & 5 can be used to connect a RS485 transceiver.

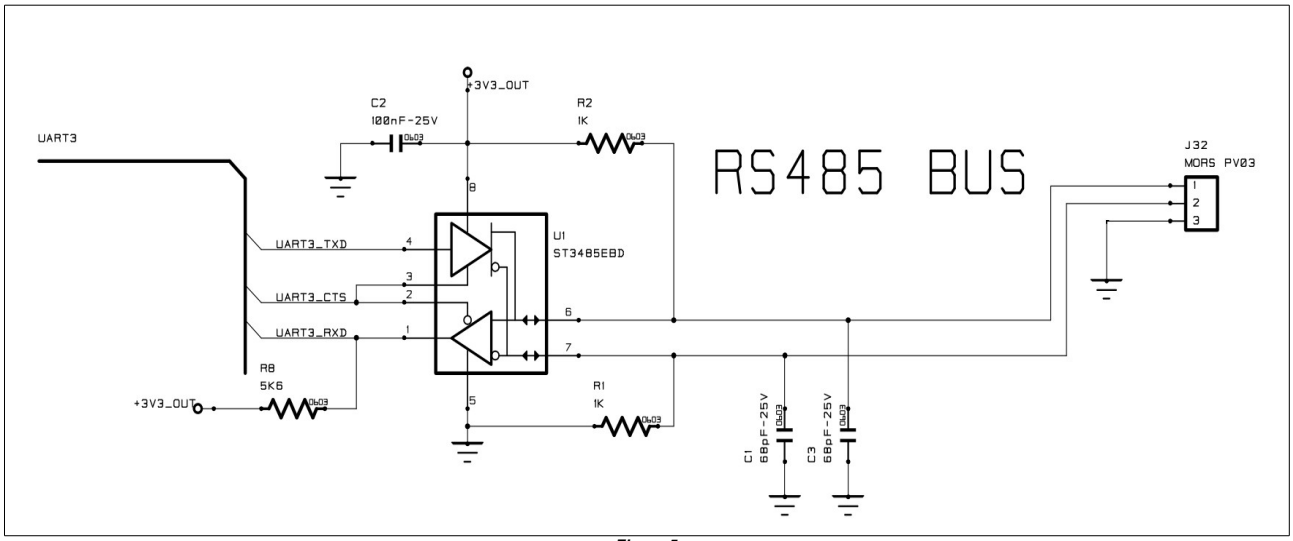


Figure 5

The pins involved in this RS485 communication example are listed in the following table.

A connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
55	UART0_CTS	UART2 CTS signal	UART2_RTS	Y	+3,3V
53	UART0_RTS	UART2 RTS signal	UART2_CTS	Y	+3,3V
49	UART0_TXD	UART2 TXD signal	UART2_TX_DATA	Y	+3,3V
51	UART0_RXD	UART2 RXD signal	UART2_RX_DATA	Y	+3,3V

Table 14

5.5 How to connect CAN BUS interfaces

In this chapter is described how CAN bus transceiver can be connected to a module. In the figure below is shown how CAN bus1 and 2 are connected in the evaluation board. Both CAN buses have been implemented.

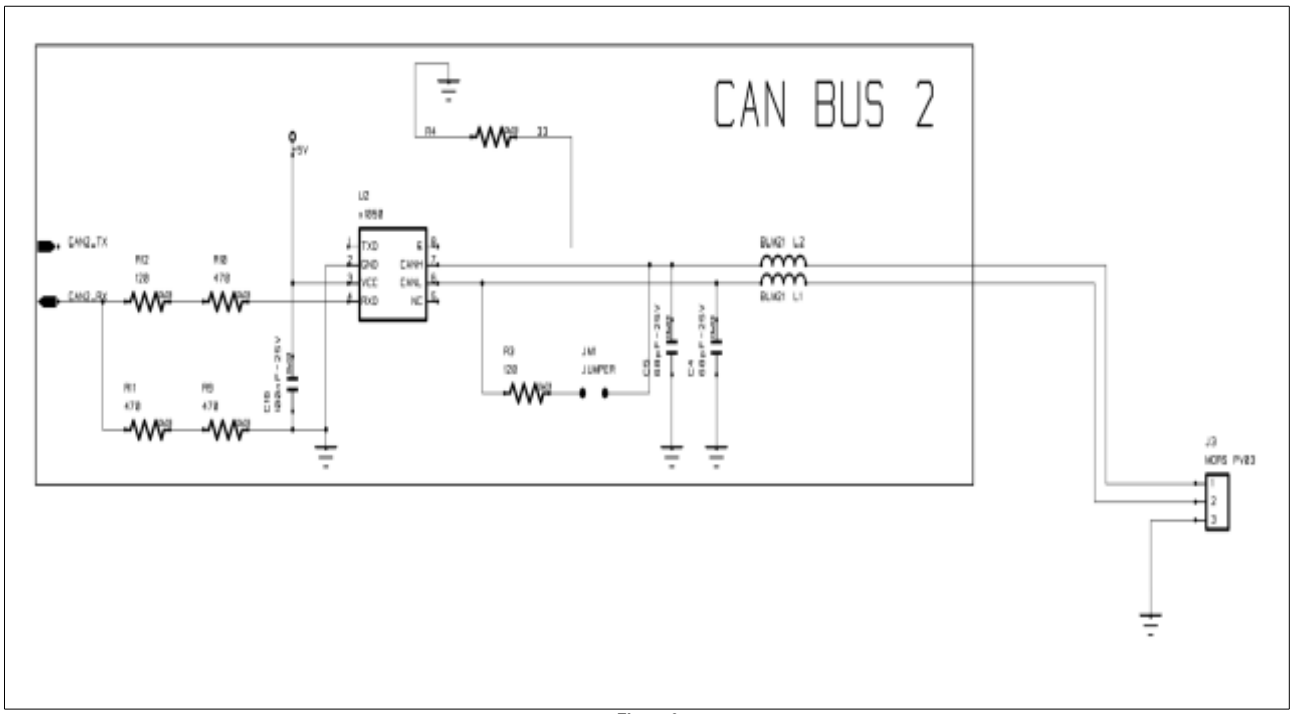


Figure 6

The following table describes the pins' numbering in the main connector involved in the CAN interface

B connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
88	CAN1_TX	CAN 1 transmit signal	UART3_CTS	Y	+3,3V
90	CAN1_RX	CAN 1 receive signal	UART3_RTS	Y	+3,3V

Table 15

The Jumpers JM1, JM5 are used to close the load of the CAN Bus to 120 Ω

5.6 How to design the Ethernet interface

The NXP i.MX6UL Ethernet Media Access Controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE standard 802.3™ networks. The 10-Mbps and 100-Mbps RMII Ethernet physical interfaces is supported. In the figure is shown how to connect the Ethernet interface to module.

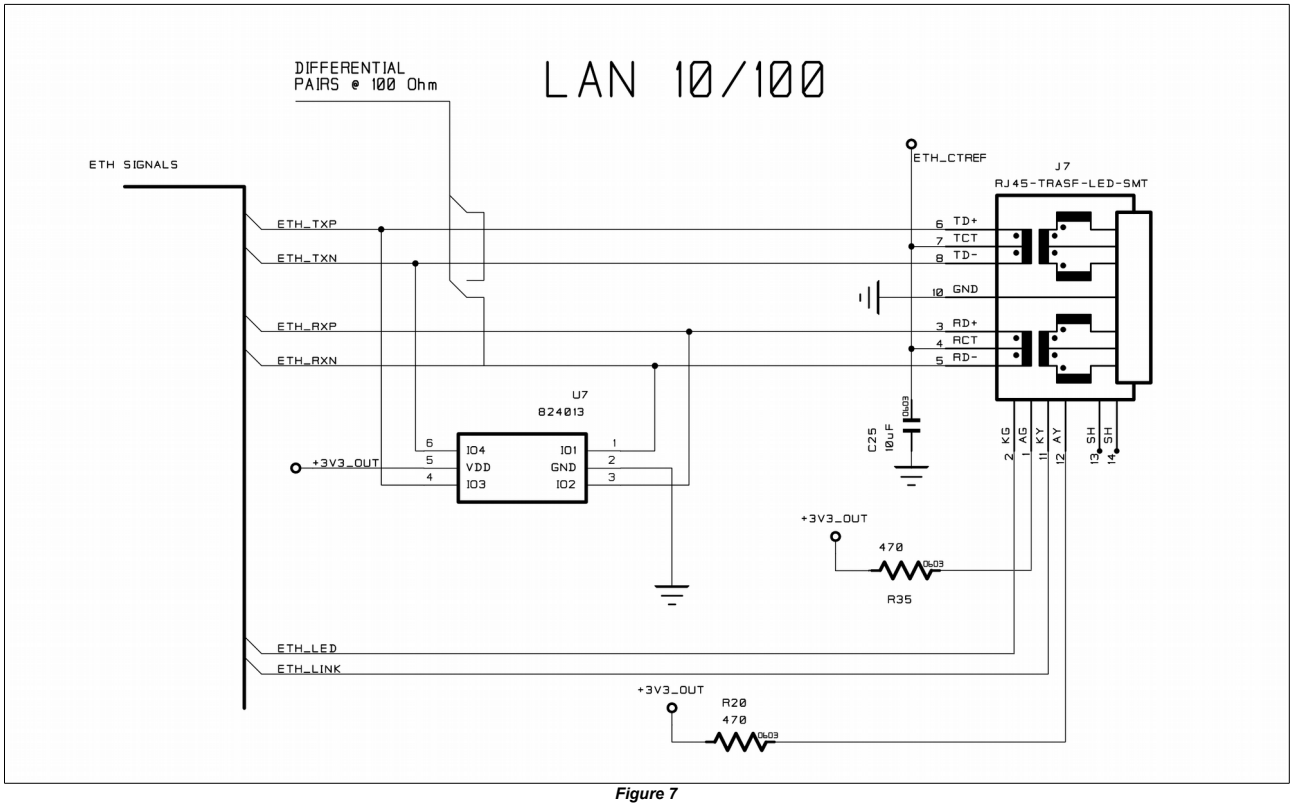


Figure 7

In the table below are listed all Ethernet signal of the module:

B Connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
33	ETH_TXN	Fast Ethernet TXN signal	-	-	+3,3V
31	ETH_TXP	Fast Ethernet TXP signal	-	-	+3,3V
39	ETH_RXN	Fast Ethernet RXN signal	-	-	+3,3V
37	ETH_RXP	Fast Ethernet RXP signal	-	-	+3,3V
35	ETH_CTREF	Mid point reference	-	-	+3,3V
41	ETH_LINK#	Led Indicator Cathode signal	-	-	+3,3V
42	ETH_ACT#	Led indicator Anode signal	-	-	+3,3V

Table 16

*** *Note:*** If not used, this pin must be left floating.

5.6.1 Component Placement considerations

Components placement can affect signal quality, emissions and can decrease EMI problems.

1. If the magnetics are a discrete component than the distance from the connector RJ45 should be kept to under 25mm of separation.
2. To decrease EMI problems the distance between magnetics and Phy should be at least 25mm or greater to isolate the PHY from magnetics.
3. The distance between Phy and RJ45 connector should always be within 200 mm.
4. The differential transmit pair should be keep at least 25mm from the edge of PCB up to the magnetics. If the magnetics are integrated into RJ45 the differential pair should be routed to the back of integrated magnetics RJ45 connector , away from the board of PCB.
5. The 49.9 ohm pull-up resistors on the differential lines should be placed within 10 mm of the Phy device
6. The signals RX & TX should be independently matched in length to within 6mm

See following figure

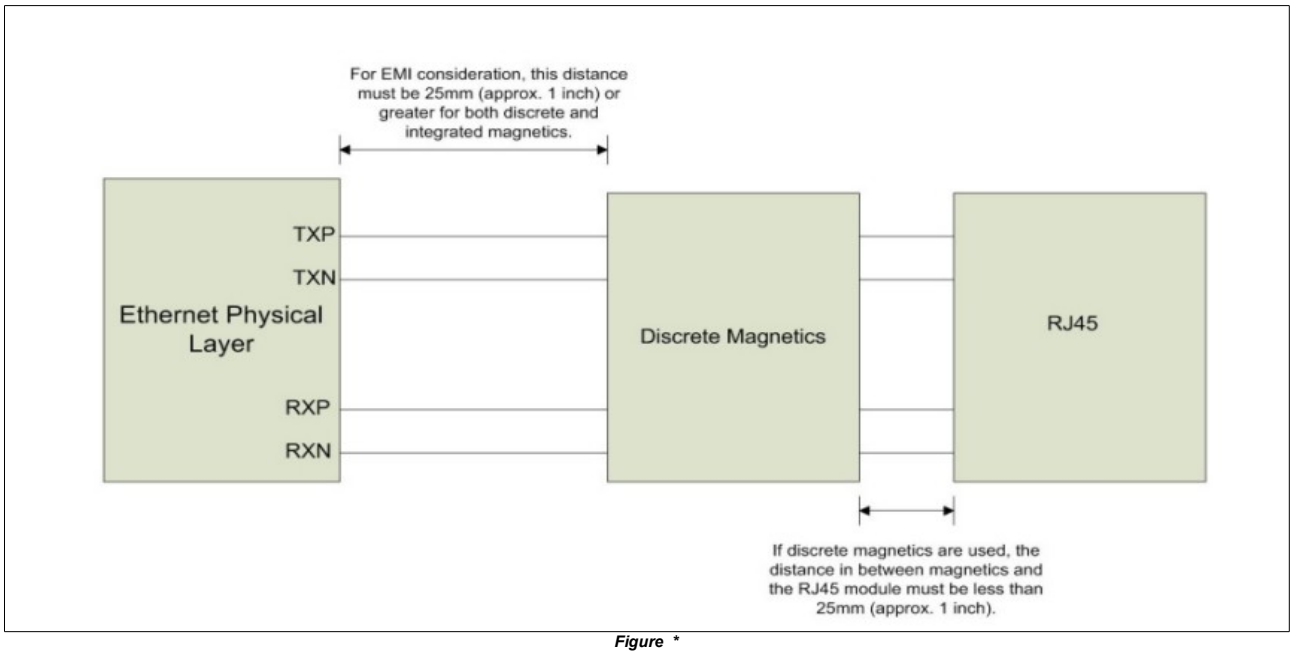


Figure *

The PHY used in the module is the ***SMSC LAN8710***.
Please for more information refer to the ***SMSC Ethernet Physical Layer Layout Guidelines***.

For a list of magnetics selected to operate with the SMSC LAN8710, please refer to the Application note ***AN 8-13 Suggested Magnetics.***

*** this is the figure 2.3 from SMSC Ethernet Physical Layer Layout Guidelines**

5.6.2 Cable Transient Event and PHY Protection

Cable transient events are + and - DC surges that are induced across the transformer onto the PHY side of the TX+/- and RX+/- signals as shown in figure below. The PHY side of the transformer should not contain any DC component other than the typical 3.3V pull-up on the center tap of the transformer for analog signal biasing. Especially in POE applications, there are two main reasons why cable transient events occur, negative rail PSE switching, and hot unplug/plug-in events.

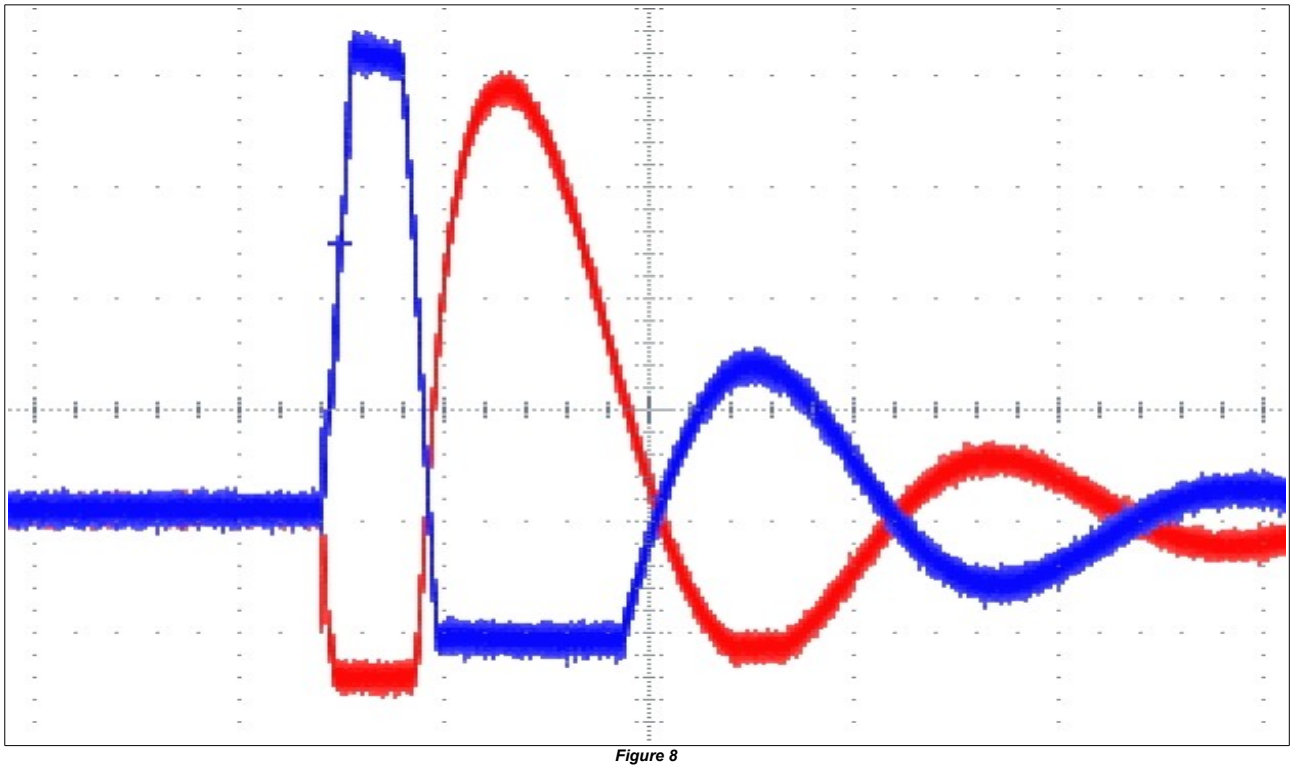


Figure 8

Transient observer on the PHY side of Eth Magnetics

Scale X = 1uS/div

Scale Y = 5V/div

Note: *for further details about Cable transient events please refers to file AN1718 of SMSC*

5.6.3 Phy Ethernet

When using an SMSC device, for each application an external transient protection is recommended , especially when the POE is used, as shown in figure below. The schematic shows an example of a TVS suppression solution. This solution couples the energy differentially into the two TVS diodes on each differential pair. For cases when the transient is across the TX+/- pair in the figure below, the voltage is clamped at a value equivalent to the forward bias voltage across D1, plus the zener voltage of D2. This transient voltage must be clamped at a voltage no **greater than 5V**. D3 and D4 act the same way when the transient is across the RX+/- differential pair. The total capacitance seen by each differential pair must not exceed 50pF (25pF single ended).

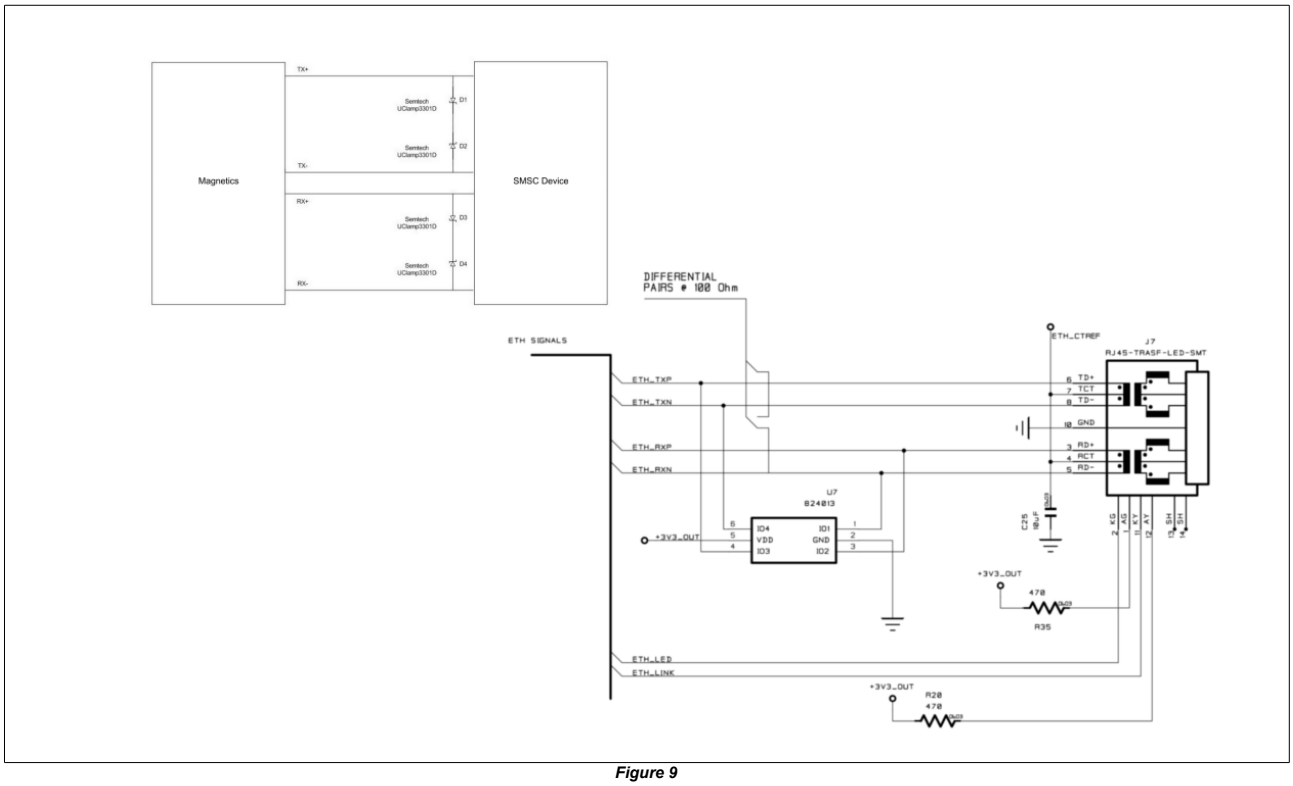


Figure 9

Recommended by ENGICAM:

Diode array TVS, 4 CH, ESD, 3.3V Wurth Elektronik 824013

Note: *for further details about PHY Protection please reffers to file AN1718 of SMSC*

5.7 USB interface

5.7.1 How to connect the USB OTG interface

The NXP i.MX6UL USB module provides high performance USB On-The-Go (up to 480Mbps), compatible with the USB 2.0 specification. An OTG HS PHY is also integrated so no external OTG PHY is needed on the baseboard. In the figure is shown how the MINI-AB USB/OTG connector is powered and connected in the evaluation board. In the following table are listed all USB/OTG signal of mail connector.

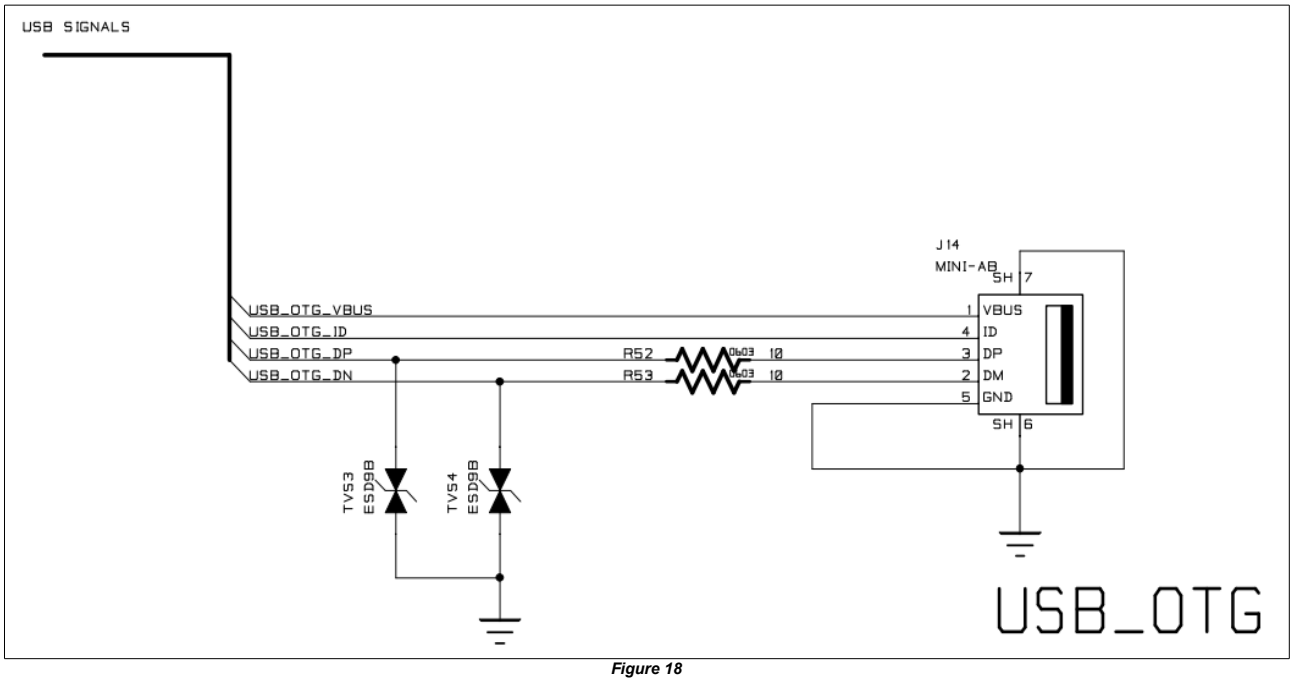


Figure 18

A connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
11	USB_OTG_VBUS *	USB on the go interface	USB_OTG1_VBUS *	N	-
13	USB_OTG_DP	USB on the go interface	USB_OTG1_DP	N	-
15	USB_OTG_DM	USB on the go interface	USB_OTG1_DN	N	-
17	USB_OTG_ID	USB on the go interface	USB_OTG1_ID	N	-

Table 17

**** Note: The USB_OTG_VBUS is an INPUT power signal. It must be connected to 5V***

In the following figures there are shown two different ways to connect the USB OTG interface that may be used to work as either a host or a device.

Use of the USB OTG port as a Host with its own dedicated supply. The ID signal is forced to GND

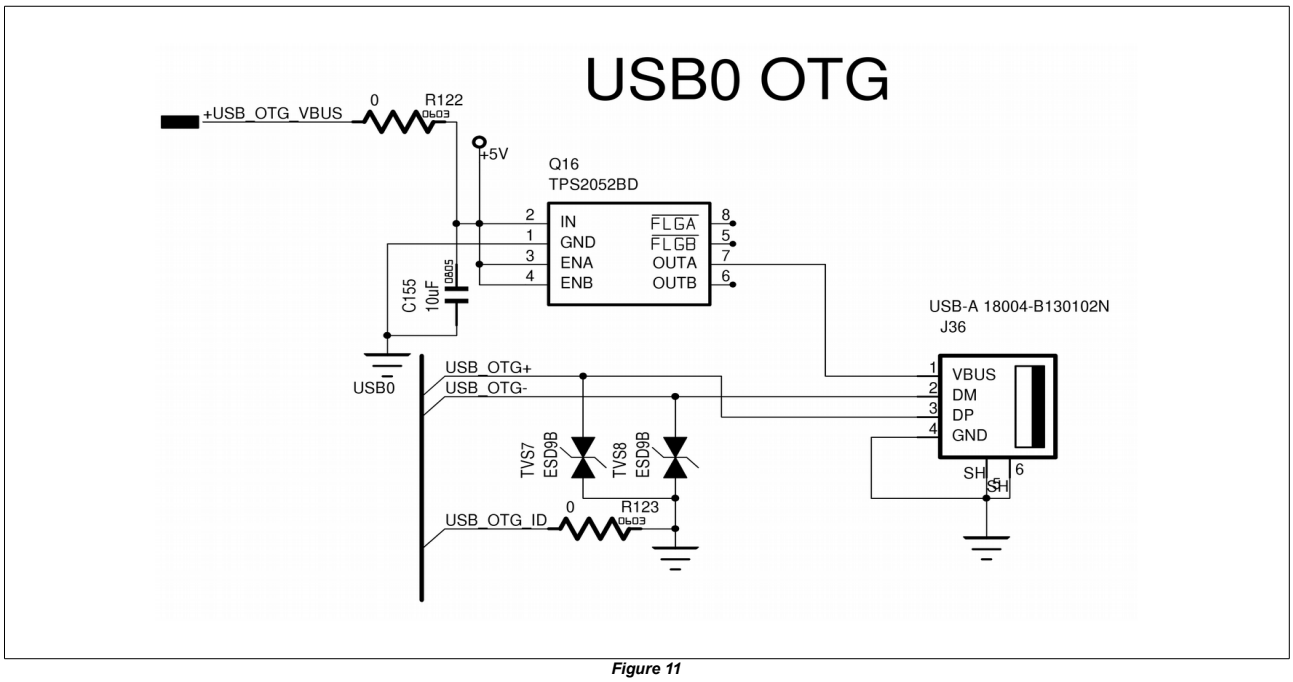


Figure 11

Use of the USB OTG port as Device or as Host depending on the status of the ID signal that is used also to enable the power supply.

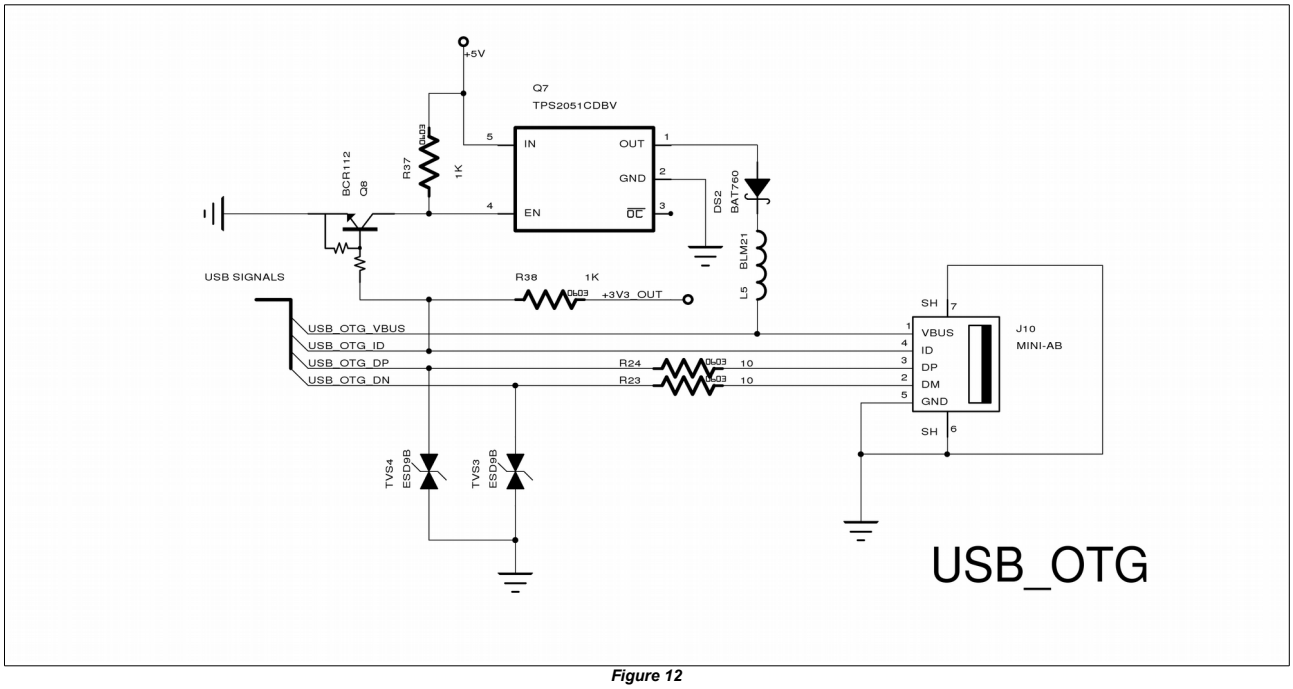


Figure 12

5.7.2 How to connect the USB host interface

The module provides one port for USB host interface. In the figure is shown how to connect this port to the Module.

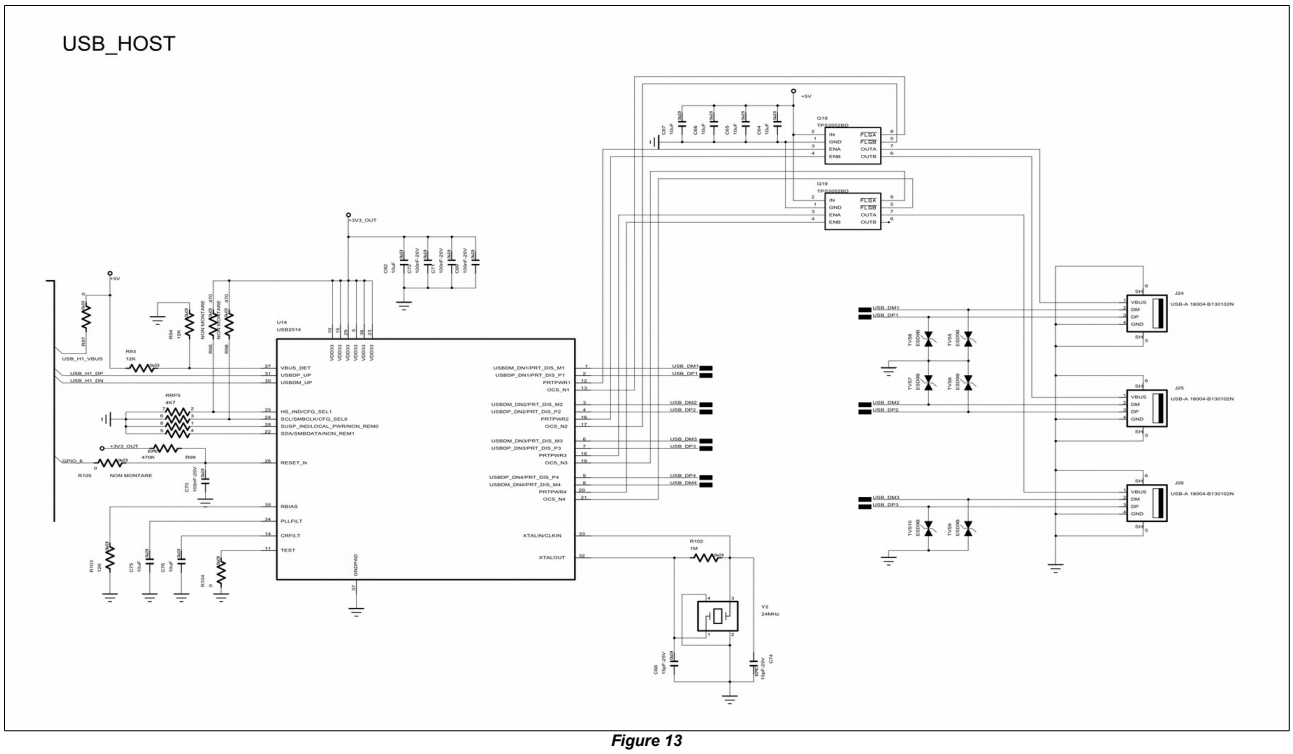


Figure 13

Engicam's evaluation board is equipped with an USB HUB to multiply the USB port available on module, if only one port is needed it's possible to connect it as one of the four output ports of the HUB output directly to module on pin 194-196 of the main connector.

B connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
2	USB_VBUS *	USB HOST interface	USB_OTG2_VBUS *	N	-
4	USB_DP	USB HOST interface	USB_OTG2_DP	N	-
6	USB_DM	USB HOST interface	USB_OTG2_DN	N	-

Table 18

**** Note: The USB_VBUS is an INPUT power signal. It must be connected to 5V***

5.8 How to connect the SD CARD interface

The NXP i.MX6UL Ultra Secured Digital Host Controller (uSDHC) provides the interface between the host system and MMC/SD/SDIO cards, including cards with reduced size or mini cards. The module include this features and in the figure is shown how the Micro SD Card connector is connected to IS.IOT Module in the evaluation board. The uSDHC signal of the module's main connector are listed in table below.

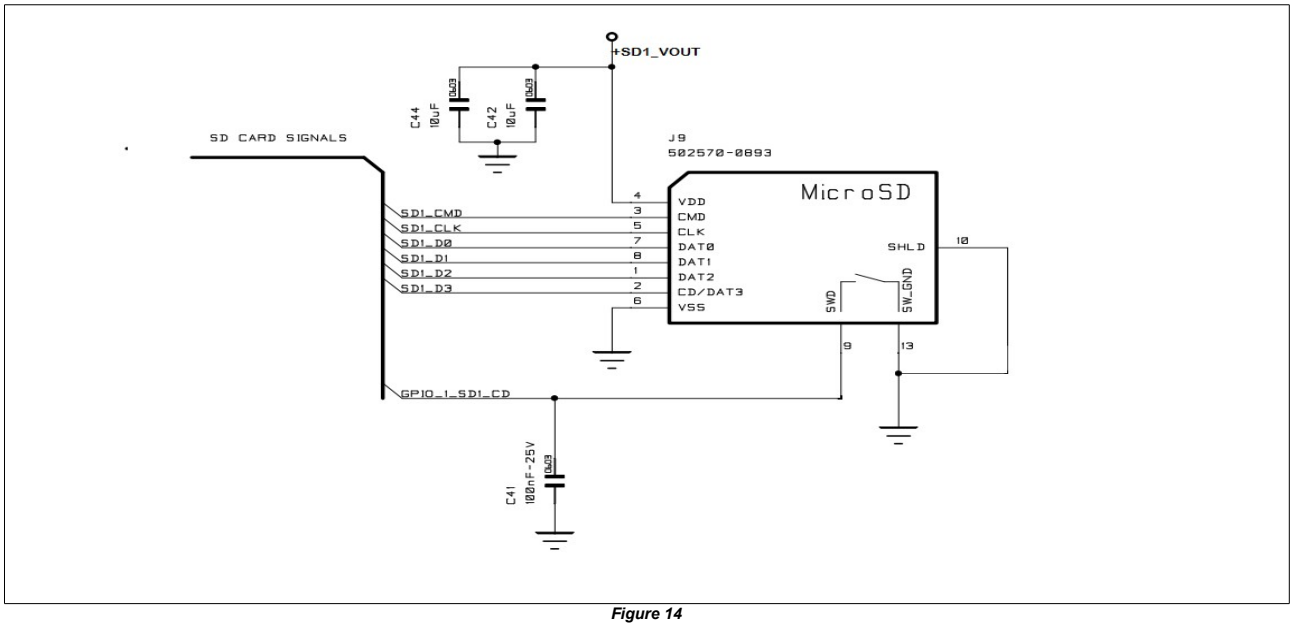


Figure 14

A Connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
26	SD1_CD	uSDHC CD Signal	UART1_RTS	Y	+3,3V
28	SD1_DAT0	uSDHC DAT 0 signal	SD1_DATA0	Y	+3,3V
30	SD1_DAT1	uSDHC DAT 1 signal	SD1_DATA1	Y	+3,3V
32	SD1_DAT2	uSDHC DAT 2 signal	SD1_DATA2	Y	+3,3V
34	SD1_DAT3	uSDHC DAT 3 signal	SD1_DATA3	Y	+3,3V
38	SD1_CLK	uSDHC CLK signal	SD1_CLK	Y	+3,3V
40	SD1_CMD	uSDHC CMD signal	SDI1_CMD	Y	+3,3V

Table 19

WARNING:
Only for the module with Wi-Fi – BT option: the SD1 signals are shared between the SDIO pins of the A connector and Wi-Fi interface. The SDIO pins are available only when nSD_BOOT signal is asserted. In this case the Wi-Fi interface is not available and SDIO signals become available for on module NAND/eMMC programming purpose.

The SD Card and Wi-Fi interfaces are enabled, by the signal "nSD_BOOT", as follow:

A Connector	Signal	LOGIC LEVEL	SD CARD	Wi-Fi
60	nSD_BOOT	0	ON	OFF
	nSD_BOOT	1	OFF	ON

Table 20

5.9 How to connect an LCD display

The evaluation board is equipped with one RGB data port, this interface contains RGB data of 18 bit, pixel clock.
Following are reported the schematic interface with parallel URT and the map of signals.

A Connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
90	LCD_CLK	LCD interface	LCD_CLK	Y	+3,3V
82	LCD_D17	LCD interface	LCD_DATA17	Y	+3,3V
80	LCD_D16	LCD interface	LCD_DATA16	Y	+3,3V
78	LCD_D15	LCD interface	LCD_DATA15	Y	+3,3V
76	LCD_D14	LCD interface	LCD_DATA14	Y	+3,3V
74	LCD_D13	LCD interface	LCD_DATA13	Y	+3,3V
72	LCD_D12	LCD interface	LCD_DATA12	Y	+3,3V
70	LCD_D11	LCD interface	LCD_DATA11	Y	+3,3V
89	LCD_D10	LCD interface	LCD_DATA10	Y	+3,3V
87	LCD_D09	LCD interface	LCD_DATA09	Y	+3,3V
85	LCD_D08	LCD interface	LCD_DATA08	Y	+3,3V
83	LCD_D07	LCD interface	LCD_DATA07	Y	+3,3V
81	LCD_D06	LCD interface	LCD_DATA06	Y	+3,3V
79	LCD_D05	LCD interface	LCD_DATA05	Y	+3,3V
77	LCD_D04	LCD interface	LCD_DATA04	Y	+3,3V
75	LCD_D03	LCD interface	LCD_DATA03	Y	+3,3V
73	LCD_D02	LCD interface	LCD_DATA02	Y	+3,3V
71	LCD_D01	LCD interface	LCD_DATA01	Y	+3,3V
69	LCD_D00	LCD interface	LCD_DATA00	Y	+3,3V
88	LCD_VSYNC	LCD interface	LCD_VSYNC	Y	+3,3V
86	LCD_HSYNC	LCD interface	LCD_HSYNC	Y	+3,3V
84	LCD_OE	LCD interface	LCD_ENABLE	Y	+3,3V

Table 21

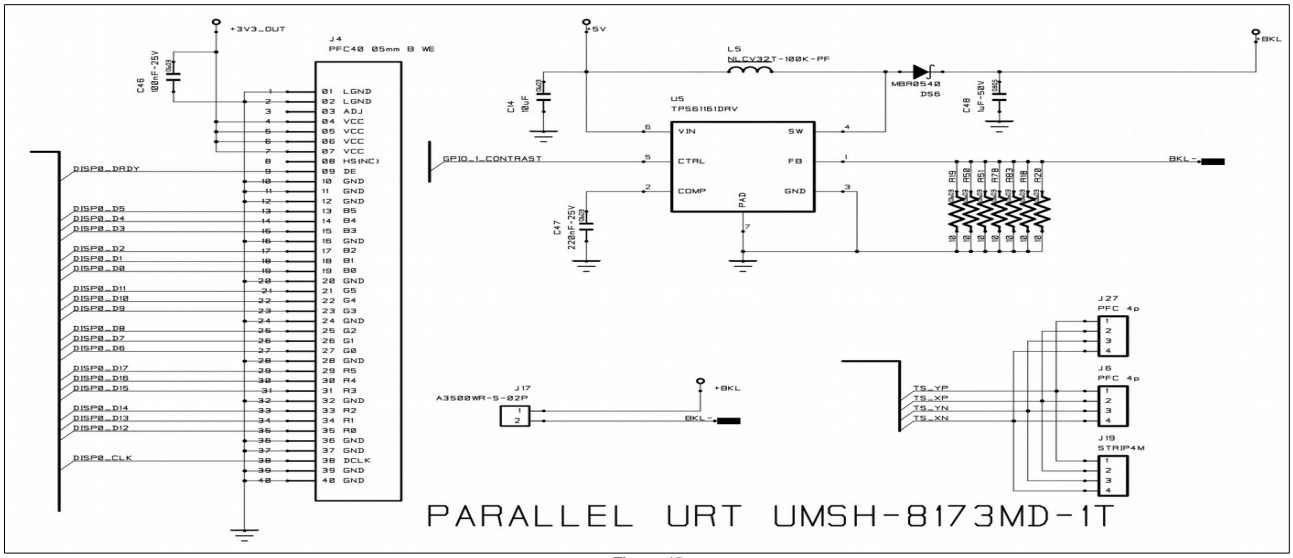


Figure 15

5.9.1 Connection map for 18 bit TFT only

The following map represent the connection mode applied to 18 bit TFT display
For every connection the colour controlled is joined

A Connector	Name	18 bit TFT connections
69	LCD_D0	BLU 0
71	LCD_D1	BLU 1
73	LCD_D2	BLU 2
75	LCD_D3	BLU 3
77	LCD_D4	BLU 4
79	LCD_D5	BLU 5
81	LCD_D6	GREEN 0
83	LCD_D7	GREEN 1
85	LCD_D8	GREEN 2
87	LCD_D9	GREEN 3
89	LCD_D10	GREEN 4
70	LCD_D11	GREEN 5
72	LCD_D12	RED 0
74	LCD_D13	RED 1
76	LCD_D14	RED 2
78	LCD_D15	RED 3
80	LCD_D16	RED 4
82	LCD_D17	RED 5

Table 22

5.10 Wi-Fi + Bluetooth Interface

The IS.IOT module is equipped with **Sterling-LWB™ 2.4 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module.** This module is based upon the **Broadcom 4343W** chipset, and supports IEEE 802.11 b/g/n, BT 2.1+EDR, and BLE 4.1 wireless connectivity. The module comes in three configurations to best address specific applications, and features an industrial temperature rating (-40° to +85° C) and an industry-leading breadth of certifications and antenna options.

Following the Wi-Fi interface pin map, it uses the pin of SDIO interface so SD card is not usable when the Wi-Fi is activated

A Connector	Name	Pin Name on i.MX	GPIO Capable	Voltage
28	SDIO_D0 [1)]	SD1_DATA0	Y	+3,3V
30	SDIO_D1 [1)]	SD1_DATA1	Y	+3,3V
32	SDIO_D2 [1)]	SD1_DATA2	Y	+3,3V
34	SDIO_D3 [1)]	SD1_DATA3	Y	+3,3V
40	SDIO_CMD [1)]	SD1_CMD	Y	+3,3V
38	SDIO_CLK [1)]	SDI1_CLK	Y	+3,3V

Table 23

[1)] **Only for the module with Wi-Fi – BT option:** the SD1 signals are shared between the SDIO pins of the A connector and Wi-Fi interface. The SDIO pins are available only when nSD_BOOT signal is asserted. In this case the Wi-Fi interface is not available and SDIO signals become available for on module NAND/eMMC programming purpose

The SD Card and Wi-Fi interfaces are enabled by the signal "nSD_BOOT", as follow:

A Connector (PIN)	Signal	LOGIC LEVEL	SD CARD	Wi-Fi
60	nSD_BOOT	0	ON	OFF
		1	OFF	ON

Table 24

The Bluetooth interface is managed using the PAD of the UART 5 on the iMX processor, but no one of this PAD is used in the IS.IOT pinout connector.

Connectors	Signal Name	Pin Name on i.MX	GPIO Capable	Voltage
-	UART5_RTS	GPIO1_IO08	N	-
-	UART5_CTS	GPIO1_IO09	N	-
-	UART5_RXD	UART5_RXD	N	-
-	UART5_TXD	UART5_TXD	N	-

Table 25

Only for the module with Wi-Fi – BT option: *as showing in the table the UART5 peripheral is used to manage Bluetooth interface. For this reason if UART5 is used as showed in chapter 6.1.6, the Bluetooth interface can not be used simultaneously. Use the UART5 only if Bluetooth is not used by application.*

5.11 Boot Mode Pin

Boot mode pin determines how the module boot. The following table listed the possible options of the boot mode:

BOOT_MODE	Action
1	Boot from memory devices
0	Boot from USB OTG

Table 26

The boot from USB OTG is usually used for the boot loader deploy.

In the figure is shown the boot section. The closing of JM2 corresponds to put at logical 1 the boot mode pin.

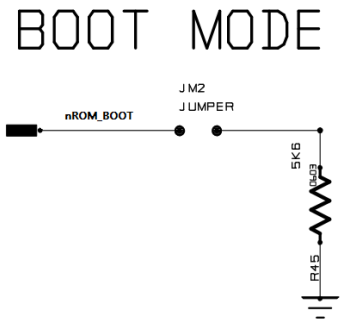


Figure 21

In Table below is listed the boot mode Pin numbering. The BOOT_MODE pins are connected to the signal nROM_BOOT pin

A Connector	Name	Primary Function Description	GPIO Capable	Voltage
58	nROM_BOOT	Boot from USB/UART or Memory device	N	-

Table 27

In the evaluation board we set-up all the configurations for bootstrap from NAND/eMMC or from SD card.

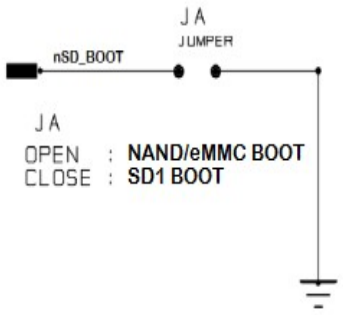


Figure 22

The figure above shows the implementation of the boot option applied to the EVABOARD. The signal used to configure the boot is implemented on pin 60. In the standard condition the signal is setting to boot from internal module memory device (jumper left open), closing the jumper the module start from SD card.

Following you can see the signals logical level to implement a custom starting sequence. The first sequence is already implemented in the module.

BOOT from Internal Module's Memory Device		
A Connector	Module Signal	LOGIC LEVEL
60	nSD_BOOT	1

Table 28

When Pin 60 is set to **high logical level**:

- if module is equipped with NAND, the boot run from NAND
- if module is equipped with eMMC, the boot run from eMMC

The NAND and eMMC **can NOT be coexist** in the IS.IOT module.

If in the module is mounted the Wi-Fi option, the boot from SD1 and its use forbids the use of Wi-Fi interface and vice versa. When the module has this setting the booting from SD1 is thought for the programming of the NAND or the eMMC during the production process.

In the module without Wi-Fi option the SD1 is always available.

BOOT FROM SD1 device		
A Connector	Module Signal	LOGIC LEVEL
60	nSD_BOOT	0

Table 29

Whatever starting sequence you chose you must consider the pin 60 of the A connector is used to the boot configuration.

WARNING:
the SD1 and Wi-Fi peripherals use the same SDIO iMX processor pin, so the use of SD1 peripheral make the Wi-Fi not working. Likewise when Wi-Fi is working the SD1 pin are not connected.

Note: for using of any customized boot options please refer to the NXP reference manual of i.MX6UL

5.11.1 Boot Signals Management

Following are shown the signals you must consider during the boot sequence:

Signal	A connector Pin number	Status on Reset (*Mandatory*)	PIN constrained on Module	Boot Config Signal	Boot eFUSE Descriptions
UART8_TXD	57	Floating	-	BOOT_CFG4[4]	
UART8_RXD	59	Floating	-	BOOT_CFG4[5]	
DISP0_D17	82	Floating	10K Ohm Pull Down	BOOT_CFG4[1]	
DISP0_D16	80	Floating	10K Ohm Pull Down	BOOT_CFG4[0]	
DISP0_D15	78	Floating	10K Ohm Pull Down	BOOT_CFG2[7]	
DISP0_D14	76	Floating	10K Ohm Pull Down	BOOT_CFG2[6]	
DISP0_D13	74	Floating	10K Ohm Pull Down	BOOT_CFG2[5]	
DISP0_D12	72	Floating	10K Ohm Pull Down	BOOT_CFG2[4]	
DISP0_D11	70	Floating	-	BOOT_CFG2[3]	
DISP0_D10	89	Floating	10K Ohm Pull Down	BOOT_CFG2[2]	
DISP0_D9	87	Floating	10K Ohm Pull Down	BOOT_CFG2[1]	
DISP0_D8	85	Floating	10K Ohm Pull Down	BOOT_CFG2[0]	
DISP0_D7	83	Floating	-	BOOT_CFG1[7]	
DISP0_D6	81	Floating	-	BOOT_CFG1[6]	
DISP0_D5	79	Floating	-	BOOT_CFG1[5]	
DISP0_D4	77	Floating	-	BOOT_CFG1[4]	
DISP0_D3	75	Floating	-	BOOT_CFG1[3]	
DISP0_D2	73	Floating	10K Ohm Pull Down	BOOT_CFG1[2]	
DISP0_D1	71	Floating	10K Ohm Pull Down	BOOT_CFG1[1]	
DISP0_D0	69	Floating	10K Ohm Pull Down	BOOT_CFG1[0]	

Table 30

The NXP documentation declares the above signals as BOOT_CFG signals but no other information (function and reset status) is currently given about them.
Basing on the Engicam test result we currently suggest to leave all these signals floating during reset status and **it's strongly recommended to consult the NXP's documentation before starting the carrier board design.**

WARNING:

The BOOT_CFG4 signals are used also to configure the boot from serial ROM, please always refer to the NXP's documentations to design and configure the listed BOOT_CFG signals of your own board

5.12 How to connect the Audio Interface

The figure shows how to connect the module I2S interface to a low-power stereo codec, e.g. NXP SGTL5000, that includes headphones and is designed to provide a comprehensive audio solution for portable products that require line-in, mic-in, line-out, headphone-out and digital I/O.

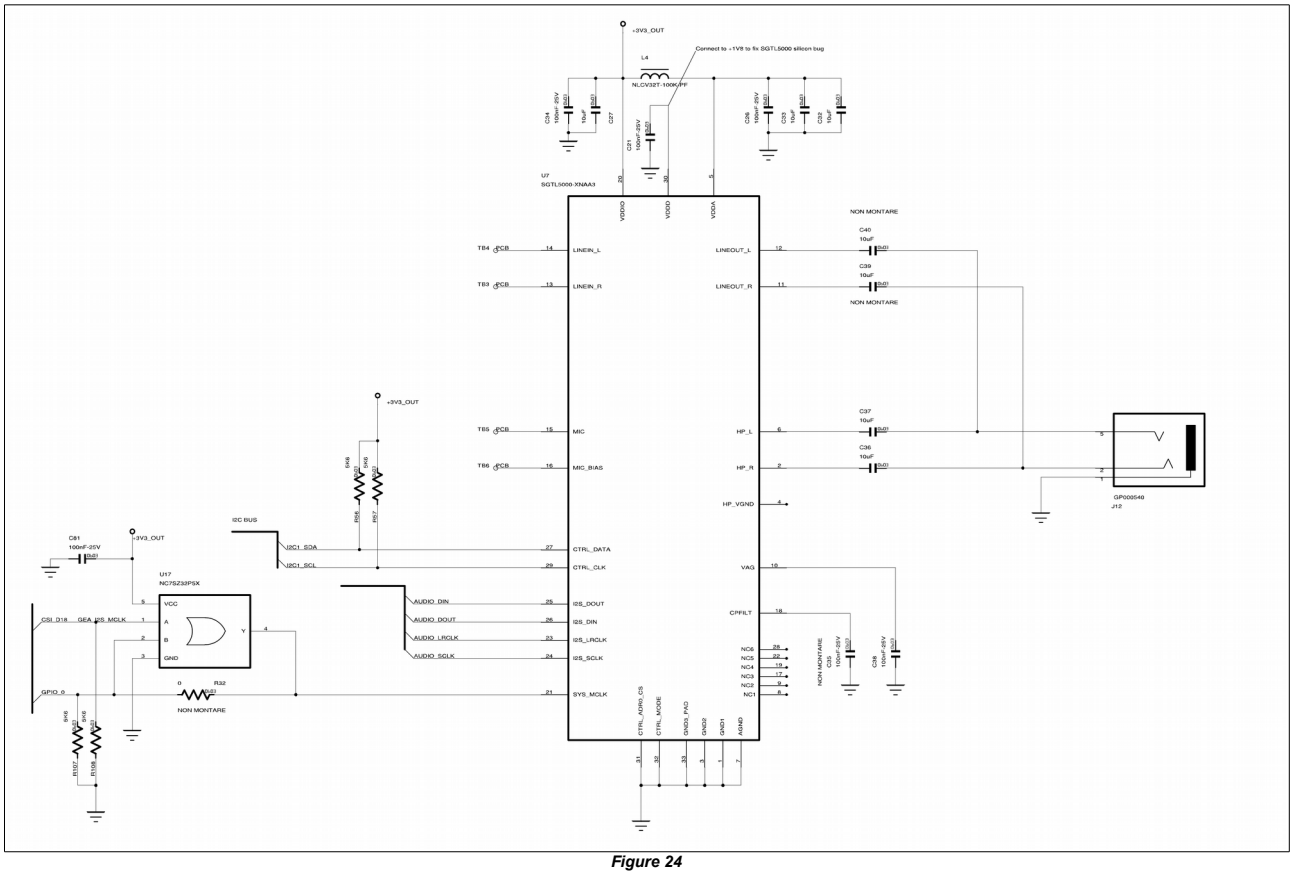


Figure 24

Following the I2S BUS pins mapping

A Connector	Name	Primary Function Description	Pin Name on i.MX	GPIO Capable	Voltage
37	I2S_IN	I2S Data In	JTAG_TCK	Y	+3,3V
39	I2S_OUT	I2S_Data OUT	JTAG_TRST_B	Y	+3,3V
35	I2S_CLK	I2S_SCLK	JTAG_TDI	Y	+3,3V
41	I2S_FRM	I2S_LRCLK	JTAG_TDO	Y	+3,3V
45	I2S_MCLK	SYS_MCLK	JTAG_TMS	Y	+3,3V

Table 31

WARNING!
To implement the SGTL5000 on the carrier board, remember to supply the VDD pin 30 of the SGTL5000 device by fixed voltage as suggested to fix a silicon bug (for further detail refer to SGTL5000 data sheet)

5.13 How to connect the reset pin

The nRESET signal has input/output functionality and shall be driven in open-drain mode. *The signal has an internal 100K pull-up and a 100 Ohm series resistors, the maximum recommended capacitive load is about* ***100pF.***

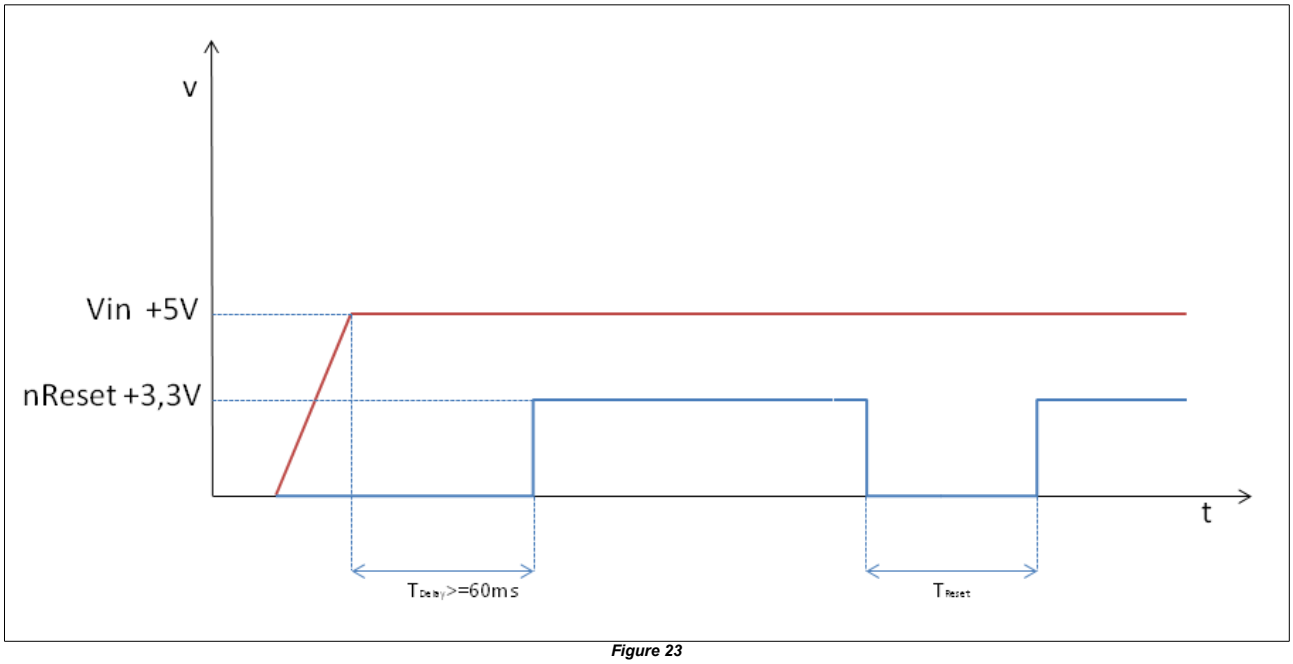


Figure 23

T_{Delay}: driven low by SOM during the POR state
T_{Reset}: driven low by user to force POR CPU pin

5.13.1 Input mode usage

The nRESET signal can be used to reset the module by driving it with an **open-drain** or with a simple button. If there are no special requirements, the module is fully auto-sufficient in terms of reset sequence, so its nRESET signal can be left floating. No Pull-up resistor is required on the carrier board; if a different pull-up resistor value (from the 100K on board of the module) is necessary, an additional pull-up on the carrier can be placed with values greater than 10K Ohm.

5.13.2 Output mode usage

The nRESET signal can also be used to monitor POR phase of the module, or to apply the reset (POR only) to other devices on the carrier. In this case, please take care to always respect limits imposed by maximum capacitive load and minimum additional pull-up.

WARNING: nReset is a POR signal only, therefore it may not be driven by the SOM during another CPU reset event (e.g. WDOG reset).

Chapter

6

6. Peripheral multiplexing

This Chapter gives the alternative peripheral informations

Section includes

- ✔ **I2S**
- ✔ **SPI**
- ✔ **PWM**
- ✔ **ADC**
- ✔ **I2C**
- ✔ **UART**
- ✔ **CSI**
- ✔ **SD**
- ✔ **CAN**

6.1 Peripheral multiplexing description

Following we describe opportunity to use alternative interfaces using the properties of multiplexing pin.
Please refer to the NXP's reference manual and documentation for further details (document name i.MX6UL Reference Manual).

6.1.1 SPI Interfaces

Using pin multiplexing 's features we may have the following SPI and IIS connections. In the tables below are shown the output signals on the Connector's module.

ECSPI1 signals interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
-	83	-	CSI_DATA06	MOSI	+3,3V
-	85	-	CSI_DATA07	MISO	+3,3V
57	79	LCD_DATA20	CSI_DATA04	SCLK	+3,3V
59	81	LCD_DATA21	CSI_DATA05	SS0	+3,3V
79	-	LCD_DATA05	-	SS1	+3,3V
81	-	LCD_DATA06	-	SS2	+3,3V
83	-	LCD_DATA07	-	SS3	+3,3V

Table 32

ECSPI2 signals interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
-	75	-	CSI_DATA02	MOSI	+3,3V
-	77	-	CSI_DATA03	MISO	+3,3V
20	71	UART4_TX_DATA	CSI_DATA00	SCLK	+3,3V
18	73	UART4_RX_DATA	CSI_DATA01	SS0	+3,3V
86	-	LCD_HSYNC	-	SS1	+3,3V
88	-	LCD_VSYNC	-	SS2	+3,3V
25	-	LCD_RESET	-	SS3	+3,3V

Table 33

ECSPI3 signals interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
27	-	NAND_CE1_B	-	MOSI	+3,3V
55		UART2_CTS_B			
53	-	UART2_RTS_B	-	MISO	+3,3V
51	-	UART2_RX_DATA	-	SCLK	+3,3V
49	-	UART2_TX_DATA	-	SS0	+3,3V

Table 34

6.1.2 IIS Configuration

The following tables show the pin configurations for IIS Bus on module's connector.

IIS1 bus interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
75	83	LCD_DATA03	CSI_DATA06	I2S_DIN	+3,3V
77	85	LCD_DATA04	CSI_DATA07	I2S_DOUT	+3,3V
73	81	LCD_DATA02	CSI_DATA05	I2S_SCLK	+3,3V
69	73	LCD_DATA00	CSI_DATA01	I2S_MCLK	+3,3V
71	79	LCD_DATA01	CSI_DATA04	I2S_LRCLK	+3,3V

Table 35

IIS2 bus interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
37	-	JTAG_TCK	-	I2S_DIN	+3,3V
32		SD1_DATA2 [1)]			
39	-	JTAG_TRST_B	-	I2S_DOUT	+3,3V
34		SD1_DATA3 [1)]			
35	-	JTAG_TDI	-	I2S_SCLK	+3,3V
30		SD1_DATA1 [1)]			
45	-	JTAG_TMS	-	I2S_MCLK	+3,3V
38		SD1_CLK [1)]			
41	-	JTAG_TDO	-	I2S_LRCLK	+3,3V
28		SD1_DATA0 [1)]			

Table 36

[1)] These pins are available only without Wi-Fi-Bluetooth option

IIS3 bus interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
76	-	LCD_DATA14	-	I2S_DIN	+3,3V
78	-	LCD_DATA15	-	I2S_DOUT	+3,3V
25		LCD_RESET			
70	-	LCD_DATA11	-	I2S_SCLK	+3,3V
90	-	LCD_CLK	-	I2S_MCLK	+3,3V
87		LCD_DATA09			
72	-	LCD_DATA12	-	I2S_LRCLK	+3,3V
84		LCD_ENABLE			

Table 37

6.1.3 Alternative PWM pins table

It's possible to set the pins shown in the following table as PWM signals.

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
69	-	LCD_DATA00	-	PWM-1	+3,3V
71	-	LCD_DATA01	-	PWM-2	+3,3V
73	79	LCD_DATA02	GPIO1_IO04	PWM-3	+3,3V
75	80	LCD_DATA03	GPIO1_IO05	PWM-4	+3,3V
66	-	NAND_DQS	-	PWM-5	+3,3V
35	-	JTAG_TDI	-	PWM-6	+3,3V
37	89	JTAG_TCK	CSI_VSYNC	PWM-7	+3,3V
19	87	ENET1_RX_ER	CSI_HSYNC	PWM-8	+3,3V
39		JTAG_TRST_B			

Table 38

6.1.4 ADC

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
-	30	-	GPIO1_IO00	ADC1_IN0	+3,3V
				ADC2_IN0	
-	28	-	GPIO1_IO01	ADC1_IN1	+3,3V
				ADC2_IN1	
-	76	-	GPIO1_IO02	ADC1_IN2	+3,3V
				ADC2_IN2	
-	78	-	GPIO1_IO04	ADC1_IN4	+3,3V
				ADC2_IN4	
-	80	-	GPIO1_IO05	ADC1_IN5	+3,3V
				ADC2_IN5	
-	82	-	GPIO1_IO06	ADC1_IN6	+3,3V
				ADC2_IN6	
-	84	-	GPIO1_IO07	ADC1_IN7	+3,3V
				ADC2_IN7	

Table 39

Please refer to the iMX reference manual for further details about ADC configuration

6.1.5 IIC Configuration

IIC1 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
20	74	UART4_TX_DATA	CSI_PIXCLK	SCL	+3,3V
	76		GPIO1_IO02		
18	72	UART4_RX_DATA	CSI_MCLK	SDA	+3,3V

Table 40

IIC2 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
-	87	-	CSI_HSYNC	SCL	+3,3V
	30		GPIO1_IO00		
-	89	-	CSI_VSYNC	SDA	+3,3V
	28		GPIO1_IO01		

Table 41

IIC3 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
71	-	LCD_DATA01	-	SCL	+3,3V
57		UART1_TX_DATA			
69	-	LCD_DATA00	-	SDA	+3,3V
59		UART1_RX_DATA			

Table 42

IIC4 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
75	-	LCD_DATA03	-	SCL	+3,3V
49		UART2_TX_DATA			
73	-	LCD_DATA02	-	SDA	+3,3V
51		UART2_RX_DATA			

Table 43

6.1.6 Alternative UART pins tables

The following tables shows an alternative UART configuration

UART1 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
26	84	UART1_RTS_B	GPIO1_IO07	UART1_CTS	+3,3V
21	82	UART1_CTS_B	GPIO1_IO06	UART1_RTS	+3,3V
54	76	UART1_TX_DATA	GPIO1_IO02	UART1_TXD	+3,3V
56	-	UART1_RX_DATA	-	UART1_RXD	+3,3V

Table 44

UART2 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
23	-	UART3_RX_DATA	-	UART2_CTS	+3,3V
53		UART2_RTS_B			
17	-	UART3_TX_DATA	-	UART2_RTS	+3,3V
55		UART2_CTS_B			
49	-	UART2_TX_DATA	-	UART2_TXD	+3,3V
51	-	UART2_RX_DATA	-	UART2_RXD	+3,3V

Table 45

UART3 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
-	90	-	UART3_RTS_B	UART3_CTS	+3,3V
27	88	NAND_CE1_B	UART3_CTS_B	UART3_RTS	+3,3V
17	-	UART3_TX_DATA	-	UART3_TXD	+3,3V
23	-	UART3_RX_DATA	-	UART3_RXD	+3,3V

Table 46

UART4 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
88	-	LCD_VSYNC	-	UART4_CTS	+3,3V
86	-	LCD_HSYNC	-	UART4_RTS	+3,3V
90	-	LCD_CLK	-	UART4_TXD	+3,3V
20		UART4_TX_DATA			
84	-	LCD_ENABLE	-	UART4_RXD	+3,3V
18		UART4_RX_DATA			

Table 47

UART5 interfaces [1)]

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
-	75	-	CSI_DATA02	UART5_CTS	+3,3V
-	77	-	CSI_DATA03	UART5_RTS	+3,3V
-	71	-	CSI_DATA00	UART5_TXD	+3,3V
	78		GPIO1_IO04		
-	73	-	CSI_DATA01	UART5_RXD	+3,3V
	80		GPIO1_IO05		

Table 48

[1)] UART5 is available only without Wi-Fi-Bluetooth option

UART6 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
-	89	-	CSI_VSYNC	UART6_CTS	+3,3V
-	87	-	CSI_HSYNC	UART6_RTS	+3,3V
-	72	-	CSI_MCLK	UART6_TXD	+3,3V
-	74	-	CSI_PIXCLK	UART6_RXD	+3,3V

Table 49

UART7 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
19	-	ENET1_RX_ER	-	UART7_CTS	+3,3V
83		LCD_DATA07			
81	-	LCD_DATA06	-	UART7_RTS	+3,3V
82	-	LCD_DATA16	-	UART7_TXD	+3,3V
80	-	LCD_DATA17	-	UART7_RXD	+3,3V

Table 50

UART8 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage reference
79	-	LCD_DATA05	-	UART8_CTS	+3,3V
77	-	LCD_DATA04	-	UART8_RTS	+3,3V
46	-	ENET2_TX_DATA1	-	UART8_TXD	+3,3V
57		UART8_TX_DATA			
48	-	ENET2_TX_EN	-	UART8_RXD	+3,3V
59		UART8_RX_DATA			

Table 51

6.1.7 Alternative CMOS Sensor Interface

CSI interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		Is.IoT Signal reference	Voltage
82	-	LCD_DATA17	-	CSI_DATA0	+3,3V
23		UART3_RX_DATA			
80	-	LCD_DATA16	-	CSI_DATA1	+3,3V
17		UART3_TX_DATA			
57	71	UART1_TX_DATA	CSI_DATA00	CSI_DATA2	+3,3V
59	73	UART1_RX_DATA	CSI_DATA01	CSI_DATA3	+3,3V
21	75	UART1_CTS_B	CSI_DATA02	CSI_DATA4	+3,3V
26	77	UART1_RTS_B	CSI_DATA03	CSI_DATA5	+3,3V
49	79	UART2_TX_DATA	CSI_DATA04	CSI_DATA6	+3,3V
51	81	UART2_RX_DATA	CSI_DATA05	CSI_DATA7	+3,3V
55	83	UART2_CTS_B	CSI_DATA06	CSI_DATA8	+3,3V
53	85	UART2_RTS_B	CSI_DATA07	CSI_DATA9	+3,3V
66	80	NAND_DQS	GPIO1_IO05	CSI_FIELD	+3,3V
-	87	-	CSI_HSYNC	CSI_HSYNC	+3,3V
-	72	-	CSI_MCLK	CSI_MCLK	+3,3V
	82		GPIO1_IO06		
-	74	-	CSI_PIXCLK	CSI_PIXCLK	+3,3V
	84		GPIO1_IO07		
-	89	-	CSI_VSYNC	CSI_ VSYNC	+3,3V

Table 52

6.1.8 SD Interfaces

SD1 [1)]

A Connector	B Connector	Pin Name on i.MX		Is.IoT Signal reference	Voltage
26	81	UART1_RTS_B	CSI_DATA05	SD1_CD	+3,3V
28	-	SD1_DATA0	-	SD1_DAT0	+3,3V
30	-	SD1_DATA1	-	SD1_DAT1	+3,3V
32	-	SD1_DATA2	-	SD1_DAT2	+3,3V
34	-	SD1_DATA3	-	SD1_DAT3	+3,3V
38	-	SD1_CLK	-	SD1_CLK	+3,3V
40	-	SDI1_CMD	-	SD1_CMD	+3,3V

Table 53

[1)] **Only for the module with Wi-Fi – BT option:** the SD1 signals are shared between the SDIO pins of the A Connector and Wi-Fi interface. The SDIO pins are available only when nSD_BOOT signal is asserted. In this case the Wi-Fi interface is not available and SDIO signals become available for on module NAND/eMMC programming purpose

SD2 [2)]

A Connector	B Connector	Pin Name on i.MX		Is.IoT Signal reference	Voltage
26	72	UART1_RTS_B	CSI_MCLK	SD2_CD	+3,3V
	84		GPIO1_IO07		
57	71	LCD_DATA20	CSI_DATA00	SD2_DAT0	+3,3V
59	73	LCD_DATA21	CSI_DATA01	SD2_DAT1	+3,3V
-	75	-	CSI_DATA02	SD2_DAT2	+3,3V
-	77	-	CSI_DATA03	SD2_DAT3	+3,3V
-	89	-	VSYNC	SD2_CLK	+3,3V
-	87	-	HSYNC	SD2_CMD	+3,3V

Table 54

[2)] ***For the module equipped with eMMC the SD2 interface is not available**. In this configuration, the pins in the table above, are always available for all the other alternative functions selectable by the processor's IOMUX, **except the SD2 peripheral** that is used for the manage of the eMMC interface.*

6.1.9 Alternatives CAN bus interfaces

CAN 1 BUS Interface

A Connector	B Connector	Pin Name on i.MX		Is.IoT Signal reference	Voltage
28	88	SD1_DATA0	UART3_CTS_B	FLEXCAN1_TX	+3,3V
85	-	LCD_DATA08	-		
30	90	SD1_DATA1	UART3_RTS_B	FLEXCAN1_RX	+3,3V
87	-	LCD_DATA09	-		

Table 55

CAN 2 BUS Interface

A Connector	B Connector	Pin Name on i.MX		Is.IoT Signal reference	Voltage
32	-	SD1_DATA2	-	FLEXCAN2_TX	+3,3V
55		UART2_CTS_B			
89		LCD_DATA11			
34	-	SD1_DATA3	-	FLEXCAN2_RX	+3,3V
53		UART2_RTS_B			
70		LCD_DATA11			

Table 56

Chapter

7

7. Is.IoT adapter - mechanical data and pinout

This Chapter gives information about board adapter dimensions and pinout specifications. The adapter allows to use the Is.IoT module in the SODIMM starterkit.

Section includes

- ✔ **Assembly Top**
- ✔ **Assembly Bottom**
- ✔ **Mechanical dimensions**
- ✔ **Pinout overview and pad specifications**

7.1 SODIMM Adapter Mechanical data

The adapter board has a standard SO DIMM footprint compliant with TYCO ELECTRONICS code 1473005-1 or compatible connector. The PCB dimensions is L 67.60 x W 39 x H 1 mm. T

7.1.1 Assembly Top View

In the following figures the board adapter size and the positioning of the IsIoT module on the board.

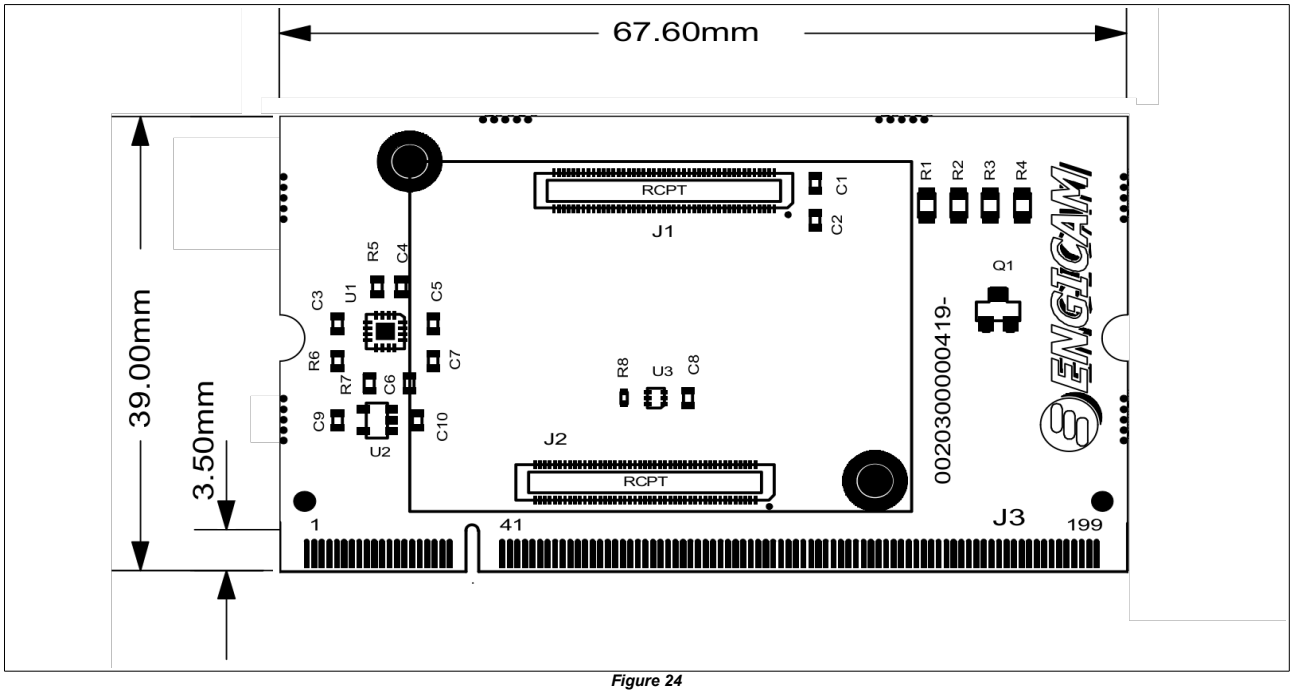


Figure 24

7.1.2 Assembly Bottom View

No components are mounted on the bottom layer of the adapter

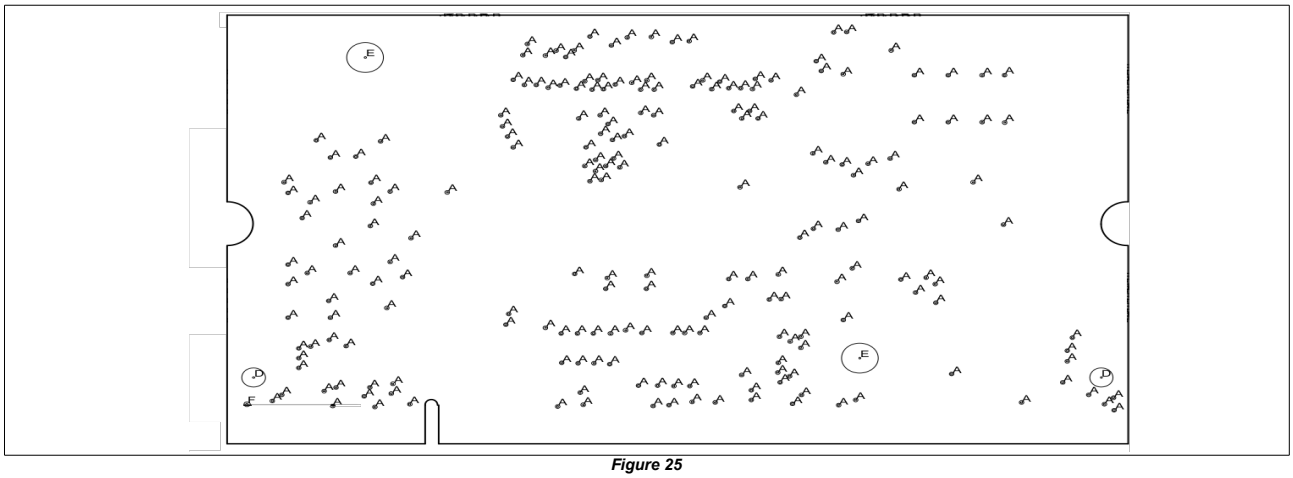


Figure 25

7.2 SODIMM Adapter Pinout

The board interface is achieved by a SO DIMM 200 position connector TYCO ELECTRONICS code 1473005-1 or compatible with the following pinout

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
1	+1V8	-	Output Power PIN	-	-
2	+1V8	-	Output Power PIN	-	-
3	GND	-	Power PIN	N	-
4	GND	-	Power PIN	N	-
5	GND	-	Power PIN	N	-
6	CSI_D[00]	CSI_DAT00	CMOS Sensor Interface Data	Y	+3,3V
7	CSI_D[11]	CSI_DAT01	CMOS Sensor Interface Data	Y	+3,3V
8	CSI_D[02]	CSI_DAT02	CMOS Sensor Interface Data	Y	+3,3V
9	CSI_D[03]	CSI_DAT03	CMOS Sensor Interface Data	Y	+3,3V
10	CSI_D[04]	CSI_DAT04	CMOS Sensor Interface Data	Y	+3,3V
11	CSI_D[05]	CSI_DAT05	CMOS Sensor Interface Data	Y	+3,3V
12	CSI_D[06]	CSI_DAT06	CMOS Sensor Interface Data	Y	+3,3V
13	CSI_D[07]	CSI_DAT07	CMOS Sensor Interface Data	Y	+3,3V
14	CSI_VSYNC	CSI_VSYNC	CMOS Sensor Interface Vertical Sync	Y	+3,3V
15	CSI_HSYNC	CSI_MCLK	CMOS Sensor Interface Horizontal Sync	Y	+3,3V
16	CSI_CLK	CSI_PIXCLK	CMOS Sensor Interface Pixel Clock	Y	+3,3V
17	NC	-	-	N	-
18	+Vcoin	VDD_SNVS_IN	Backup battery or RTC	-	-
19	NC	-	-	-	-
20	NC	-	-	-	-
21	NC	-	-	-	-
22	GND	-	Power PIN	N	-
23	I2C1_SCL	UART4_TX_DATA	I2C SCL Signal	Y	+3,3V
24	I2C1_SDA	UART4_RX_DATA	I2C SDA Signal	Y	+3,3V
25	TOUCH_XP	-	Touch Screen Xp	-	+3,3V
26	TOUCH_XN	-	Touch Screen Xn	-	+3,3V
27	TOUCH_YP	-	Touch Screen Yp	-	+3,3V
28	TOUCH_YN	-	Touch Screen Yn	-	+3,3V
29	NC	-	-	-	-
30	NC	-	-	-	-
31	GND	-	Power PIN	N	-
32	NC	-	-	-	-
33	-	-	-	-	+3,3V
34	AUD_MCLK	JTAG_TMS		Y	+3,3V
35	GPIO_1	UART3_DX_DATA	Generic GPIO	Y	+3,3V
36	GPIO_2	LCD_RESET	Generic GPIO	Y	+3,3V

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
37	GPIO_3	NAND_CE1	Generic GPIO	Y	+3,3V
38	GPIO_4	SNVS_TAMPER0	Generic GPIO	Y	+3,3V
39	GND	-	Power PIN	-	-
40	GPIO_5	SNVS_TAMPER1	Generic GPIO	Y	+3,3V
41	NC	-	-	-	-
42	NC	-	-	-	-
43	NC	-	-	-	-
44	NC	-	-	-	-
45	NC	-	-	-	-
46	NC	-	-	-	-
47	NC	-	-	-	-
48	NC	-	-	-	-
49	NC	-	-	-	-
50	NC	-	-	-	-
51	NC	-	-	-	-
52	NC	-	-	-	-
53	NC	-	-	-	-
54	NC	-	-	-	-
55	NC	-	-	-	-
56	NC	-	-	-	-
57	NC	-	-	-	-
58	NC	-	-	-	-
59	NC	-	-	-	-
60	NC	-	-	-	-
61	NC	-	-	-	-
62	NC	-	-	-	-
63	GPIO01_IO07	GPIO01_IO07	Generic GPIO	Y	+3,3V
64	GND	-	Power PIN	N	-
65	NC	-	-	-	-
66	GPIO_6	SNVS_TAMPER2	Generic GPIO	Y	+3,3V
67	NC	-	-	-	-
68	GPIO01_IO07	GPIO01_IO07	Generic GPIO	Y	+3,3V
69	NC	-	-	-	-
70	NC	-	-	-	-
71	GND	-	Power PIN	N	-
72	NC	-	-	-	-
73	NC	-	-	-	-
74	NC	-	-	-	-
75	NC	-	-	-	-
76	NC	-	-	-	-

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
77	NC	-	-	-	-
78	NC	-	-	-	-
79	NC	-	-	-	-
80	nSD_BOOT	BOOT_SEL1	External Interface Module	Y	+3,3V
81	NC	-	-	-	-
82	NC	-	-	-	-
83	NC	-	-	-	-
84	NC	-	-	-	-
85	NC	-	-	-	-
86	NC	-	-	-	-
87	NC	-	-	-	-
88	NC	-	-	-	-
89	GND	-	Power PIN	N	-
90	NC	-	-	-	-
91	NC	-	-	-	-
92	NC	-	-	-	-
93	NC	-	-	-	-
94	NC	-	-	-	-
95	NC	-	-	-	-
96	NC	-	-	-	-
97	NC	-	-	-	-
98	NC	-	-	-	-
99	NC	-	-	-	-
100	NC	-	-	-	-
101	NC	-	-	-	-
102	NC	-	-	-	-
103	NC	-	-	-	-
104	NC	-	-	-	-
105	UART0_RTS	UART2_RTS_B	UART3 CTS signal	Y	+3,3V
106	UART0_CTS	UART2_CTS_B	UART3 RTS signal	Y	+3,3V
107	GND	-	Power PIN	N	-
108	UART0_TXD	UART2_TX_DATA	UART3 TXD signal	Y	+3,3V
109	UART0_RXD	UART2_RX_DATA	UART3 RXD signal	Y	+3,3V
110	I2C2_SDA	GPIO01_IO01	I2C SDA Signal	Y	+3,3V
111	I2C2_SCL	GPIO01_IO00	I2C SCL Signal	Y	+3,3V
112	UART2_TXD	LCD_DATA20	UART2 TXD signal	Y	+3,3V
113	UART2_RXD	LCD_DATA21	UART2 RXD signal	Y	+3,3V
114	I2S_DIN	JTAG_TCK	I2S Data In	Y	+3,3V
115	I2S_LRCLK	JTAG_TDO	I2S RCLK	Y	+3,3V
116	UARTCON_TX	UART1_TX_DATA	UART4 TXD signal	Y	+3,3V

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
117	UARTCON_RX	UART1_RX_DATA	UART4 RXD signal	Y	+3,3V
118	CAN1_TX	UART3_CTS_B	CAN 1 transmit signal	Y	+3,3V
119	CAN1_RX	UART3_RTS_B	CAN 1 receive signal	Y	+3,3V
120	GPIO01_IO06	GPIO01_IO06	Generic GPIO	Y	+3,3V
121	GPIO01_IO05	GPIO01_IO05	Generic GPIO	Y	+3,3V
122	I2S_DOUT	JTAG_TRST_B	I2S Data Out	Y	+3,3V
123	GND	-	Power PIN	N	-
124	I2S_SCLK	JTAG_TDI	I2S SCLK	Y	+3,3V
125	DISP0_CLK	LCD_CLK	LCD interface	Y	+3,3V
126	NC	-	-	-	-
127	ETH0_TXN	-	Fast Ethernet TXN signal	-	-
128	nRESET	POR_B	Reset signal	N	+3,3V
129	ETH0_TXP	-	Fast Ethernet TXP signal	-	-
130	NC	-	-	-	-
131	ETH0_RXN	-	Fast Ethernet RXN signal	-	-
132	DISP0_CONTRAST	ENET1_RX_ER	LCD interface	Y	+3,3V
133	ETH0_RXP	-	Fast Ethernet RXP signal	-	-
134	+3V3_OUT	-	Output Power PIN	N	-
135	+3V3_OUT	-	Output Power PIN	N	-
136	NC	-	-	-	-
137	ETH0_LED_10_100_KATHOD	-	Led Indicator Cathode signal	-	-
138	+3V3_OUT	-	Output Power PIN	-	-
139	ETH0_LED_ACT_ANOD	-	Led indicator Anode signal	-	-
140	NC	-	-	-	-
141	DISP0_D17	LCD_DATA17	LCD interface	Y	+3,3V
142	DISP0_D16	LCD_DATA16	LCD interface	Y	+3,3V
143	DISP0_D15	LCD_DATA15	LCD interface	Y	+3,3V
144	DISP0_D14	LCD_DATA14	LCD interface	Y	+3,3V
145	DISP0_D13	LCD_DATA13	LCD interface	Y	+3,3V
146	DISP0_D12	LCD_DATA12	LCD interface	Y	+3,3V
147	DISP0_D11	LCD_DATA11	LCD interface	Y	+3,3V
148	DISP0_D10	LCD_DATA10	LCD interface	Y	+3,3V
149	DISP0_D9	LCD_DATA09	LCD interface	Y	+3,3V
150	DISP0_D8	LCD_DATA08	LCD interface	Y	+3,3V
151	DISP0_D7	LCD_DATA07	LCD interface	Y	+3,3V
152	DISP0_D6	LCD_DATA06	LCD interface	Y	+3,3V
153	DISP0_D5	LCD_DATA05	LCD interface	Y	+3,3V
154	DISP0_D4	LCD_DATA04	LCD interface	Y	+3,3V
155	DISP0_D3	LCD_DATA03	LCD interface	Y	+3,3V
156	GND	-	Power PIN	N	-

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
157	DISP0_D2	LCD_DATA02	LCD interface	Y	+3,3V
158	DISP0_D1	LCD_DATA01	LCD interface	Y	+3,3V
159	DISP0_D0	LCD_DATA00	LCD interface	Y	+3,3V
160	DISP0_VSYNC	LCD_VSYNC	LCD interface	Y	+3,3V
161	DISP0_HSYNC	LCD_HSYNC	LCD interface	Y	+3,3V
162	DISP0_DRDY	LCD_OE	LCD interface	Y	+3,3V
163	NC	-	-	-	-
164	NC	-	-	-	-
165	NC	-	-	-	-
166	GPIO01_IO04	GPIO01_IO04	Generic GPIO	Y	+3,3V
167	eCSPI4_MOSI	ENET2_TX_EN	Enhanced Configurable SPI Interface MOSI	Y	+3,3V
168	eCSPI4_MISO	ENET2_TX_CLK	Enhanced Configurable SPI Interface MISO	Y	+3,3V
169	eCSPI4_SCLK	ENET2_TX_DATA1	Enhanced Configurable SPI Interface CLK	Y	+3,3V
170	GPIO01_IO01	GPIO01_IO0	Generic GPIO	Y	+3,3V
171	eCSPI4_SS0	ENET2_RX_ER	Enhanced Configurable SPI Interface CS	Y	+3,3V
172	NC	-	-	-	-
173	NC	-	-	-	-
174	NC	-	-	-	-
175	NC	-	-	-	-
176	NC	-	-	-	-
177	NC	-	-	-	-
178	NC	-	-		-
179	NC	-	-	-	-
180	USB_H1_VBUS	USB_OTG2_VBUS	USB HOST interface	N	-
181	BOOT_MODE	-	Boot from USB UART or on board Nand Flash	-	-
182	GND	-	Power PIN	N	-
183	SDIO_DET		eSDHC CD Signal	Y	+3,3V
184	PWMO		eSDHC WP Signal	Y	+3,3V
185	SD1_D2	SD1_DATA2	uSDHC DAT 2 signal	Y	+3,3V
186	SD1_D3	SD1_DATA3	uSDHC DAT 3 signal	Y	+3,3V
187	SD1_D1	SD1_DATA1	uSDHC DAT 1 signal	Y	+3,3V
188	SD1_D0	SD1_DATA0	uSDHC DAT 0 signal	Y	+3,3V
189	SD1_CLK	SD1_CLK	uSDHC CLK signal	Y	+3,3V
190	SD1_CMD	SD1_CMD	uSDHC CMD signal	Y	+3,3V
191	USB_OTG_ID	USB_OTG1_ID	USB on the go interface	Y	+3,3V
192	USB_OTG_DP	USB_OTG1_DP	USB on the go interface	N	-
193	USB_OTG_DN	USB_OTG1_DN	USB on the go interface	N	-
194	USB_H1_DP	USB_OTG2_DP	USB HOST interface	N	-

Pin	Name	Pin Name on CPU	Primary Function Description	GPIO Capable	Voltage
195	USB_OTG_VBUS	USB_OTG1_VBUS	USB on the go interface	N	-
196	USB_H1_DN	USB_OTG2_DN	USB HOST interface	N	-
197	+5Vin	-	Power PIN	N	-
198	+5Vin	-	Power PIN	N	-
199	+5Vin	-	Power PIN	N	-
200	+5Vin	-	Power PIN	N	-

Table 57

On-line Support

We offer an on-line support to allow the customer to stay updated on the development of software release and on the enhancement of the documentation.

Following is shown the references for ENGICAM on-line support.

ENGICAM Product Experts are available to answer questions via email:

support@engicam.com

Product Compliance

In order to respect own internal policy regarding the environmental regulations and safety laws, Engicam confirms the compliant, of this product to the normatives ROHS and REACH and to the recognized hazards.

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