SMARCORE EHL HW MANUAL

SMARC Version 2.1 Compliant

REVISION HISTORY

DATE	REVISION	CHANGE DESCRIPTION
25/04/2021	1.0.0	Release
23/06/2021	1.0.1	Ordering number upgrading
24/08/2021	1.0.2	Replaced new Logo on header, added ordering codes, fixed typo error on the features table
23/08/2022	1.0.3	Fixed typo issue on Ethernet chapter
18/11/2022	1.0.4	Corrected refuse on pinout
01/12/2022	1.0.5	Added I2C slave address
14/12/2022	1.0.6	Corrected refuse on USB
19/12/2022	1.0.7	Updated to Rev.C
03/03/2023	1.0.8	Update GPIOs table. Update ordering code
23/05/2023	1.0.9	Updated I2C slave addresses
01/06/2023	1.1.0	Corrected refuse on pinout; corrected refuse on USB chapter
14/06/2023	1.1.1	Added GPIOs capable warning

TABLE OF CONTENTS

CHAPTER 1

1.INTRODUCTION

This Chapter gives background information on this document.
Section includes：

- **Acronyms and Abbreviations Used**
- **Signal Table Terminology**
- **Document and Standard References**

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

Cells with grey text contain information that is not supported on this board.

This document also contains samples reference schematics for different interfaces.

SMARC EHL module may not feature the full set of all interfaces that defined in SMARC specification.

An evaluation carrier is available for SMARC EHL computer on module.

All examples of this document are based on SMARC EHL carrier board that is available from ENGICAM. This document also provides a collection of useful documentation, application reports, and design recommendations.

The last part of the document reports the main features of the BIOS setup.

1.1 ACRONYMS AND ABBREVIATIONS USED

The table below shows the acronyms and abbreviations used in the manual.

ABBREVIATION	EXPLANATION
ADC	Analogue to Digital Converter
Auto-MDIX	Automatically Medium Dependent Interface Crossing, a PHY with Auto-MDIX f is able to detect whether RX and TX need to be crossed (MDI or MDIX)
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CPU	Central Processor Unit
DAC	Digital to Analogue Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor
DSI	Display Serial Interface
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic- sensitive devices
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
HDA	High Definition Audio (HD Audio), digital audio interface between CPU and audio codec
HDMI	High-Definition Multimedia Interface, combines audio and video signal
I2C	Inter-Integrated Circuit, two wire interfaces for connecting low speed peripherals
I2S	Integrated Interchain Sound, serial bus for connecting PCM audio data between two devices
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signalling, electrical interface standard that can transport very high speed signals over twisted-pair cables.
MSB	Most Significant Bit
NA	Not Available
NC	Not Connected
OD	Open Drain
PCB	Printed Circuit Board
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, colour channels in common display interfaces
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SOC	System on a Chip, IC which integrates the main component of a computer on a single chip
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
USB	Universal Serial Bus, serial interface for internal and external peripherals

1.2 SIGNAL TABLE TERMINOLOGY

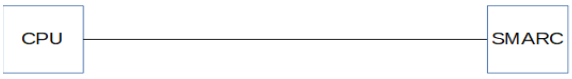
The Table below describes the terminology used in this section for the Signal Description tables.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

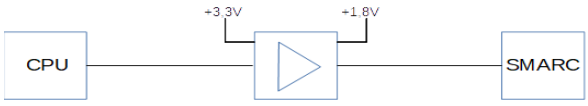
DIRECTION	TYPE	NOTE
Input		Input to the Module
Output		Output from the Module
Output OD		Open drain output from the Module
Bi-Dir		Bi-directional signal (can be input or output)
Bi-Dir OD		Bi-directional signal; output from the Module is open drain
Diff100		Differential 100 Ohm
Diff90		Differential 90 Ohm
	VDD_IN	Module input voltage
	CMOS 1.8V	CMOS logic input and / or output, 1.8V I/O supply level or tolerance
	CMOS 3.3V	CMOS logic input and / or output, 3.3V I/O supply level or tolerance
	CMOS VDD_IO	CMOS logic I/O level – set to 1.8V for SMARC EHL
	CMOS VDD_JTAG_IO	VDD_JTAG_IO is 1.8V in SMARC EHL. The JTAG emulator adjusts to the VDD_JTAG_IO level provided by the Module, on the JTAG connector
	GBE MDI	Differential analog signalling for Gigabit Media Dependent Interface
	LVDS AFB	LVDS signalling for AFB – may be PCIe, SATA, USB SS, GBE MDI, MLB or other low voltage high speed differential physical interface

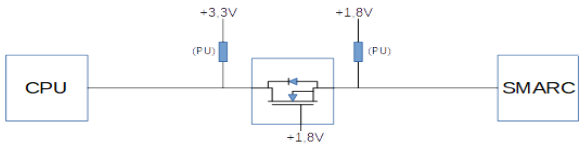
Schematics reference for GPIO configurations and level translation

GPIO Capable



Output signal





GPIO LTD (PU value)

1.3 DOCUMENT AND STANDARD REFERENCES

1.3.1 EXTERNAL INDUSTRY STANDARD DOCUMENTS

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now INTEL) (www.INTEL.com).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now INTEL) (www.INTEL.com).
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org).
- PICMG® EEEP Embedded EEPROM Specification, Rev. 1.0, August 2010 (www.picmg.org).
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org).
- SPI Bus – "Serial Peripheral Interface" - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).
- USB Specifications (www.usb.org).

1.3.2 SGET DOCUMENTS

SMARC_Hardware_Specification version 2.1, March 23, 2020.

1.4 NON-INTENDED USE

WARNING

Use the SMARC module in the specified temperature ranges only!
Use the SMARC module in the specified humidity ranges only!

1.5 ELECTROSTATIC SENSITIVE DEVICE

The ENGICAM SMARC module is an electrostatic sensitive device and it is packed accordingly.

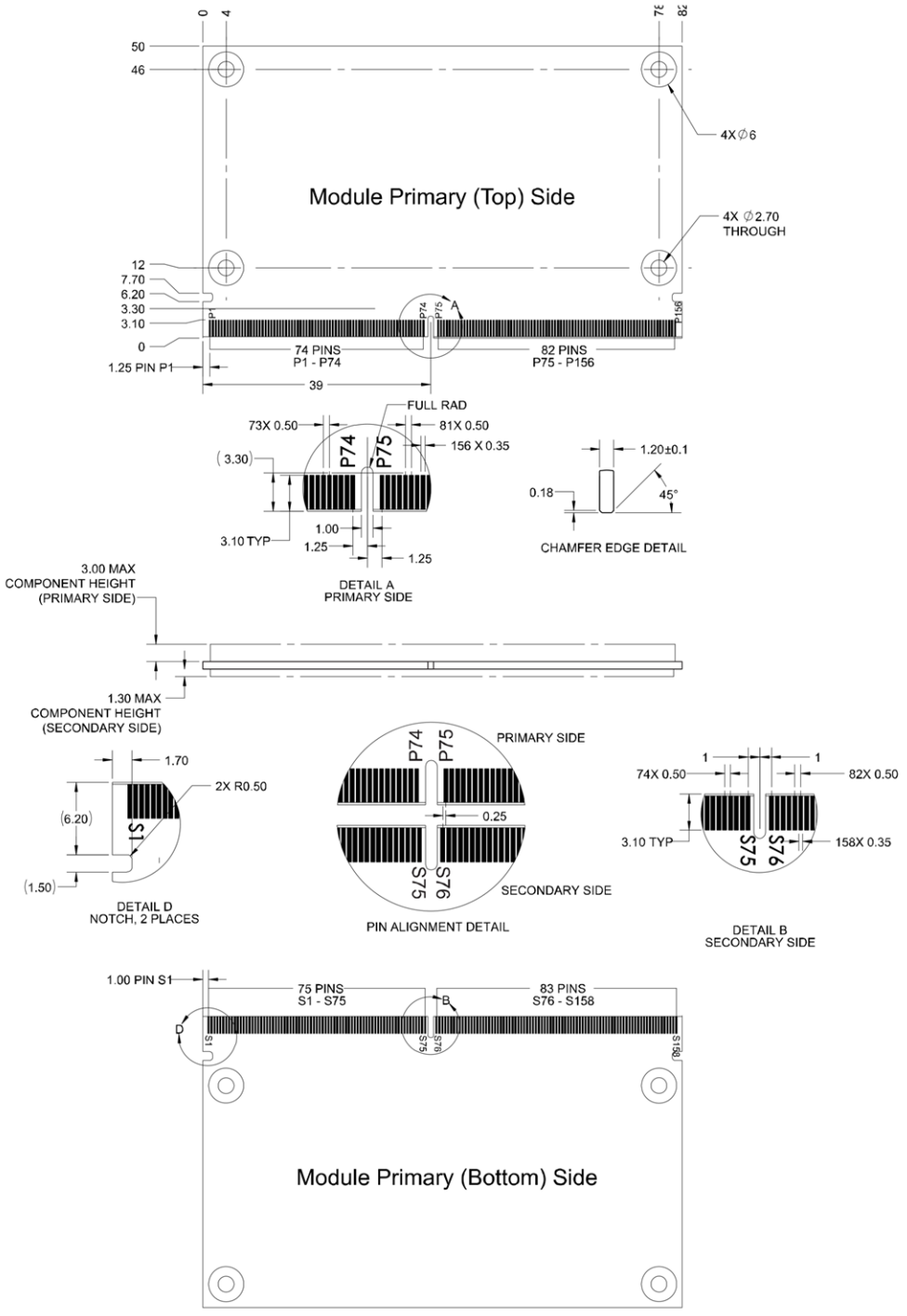
Warning:

Handle the SMARC Module at electrostatic-free workstations only.

Do not handle or store the SMARC Module near strong electrostatic, electromagnetic, magnetic or radioactive fields unless the SMARC Module is contained within its original packaging.

1.6 MECHANICAL DEFINITIONS

Engicam SMARC EHL module respects SGET SMARC mechanical definitions. Figure below comes from SMARC_Hardware_Specification version 2.1.



CHAPTER 2

2.ORDERING INFORMATION

This Chapter gives the ordering information and technical specifications of the modules.

Section includes：

- **Ordering codes**
- **CPU & Memory specifications**
- **Operating temperature range**

2.1 ORDERING INFORMATION

Following are provided the ordering information and the description of the basic technical specifications for the modules:

Marking Code	Ordering Code	MPQ	Description	CPU & Memory specifications	Operating temperature range °C (excepted CPU)[2)]	Module available at least until [1)]
SmarCore EHL X6211E 8GB	**0026800251E77A**	1	SMARC 2.**1** short size, Intel EHL X6211E, 8GB LPDDR4, 32GB **eMMC -25°C**[3)], LVDS, DUAL GB ethernet	Intel Atom X6212E dual core 6W 1.2 GHz, 1.5MB L2 cache, Industrial, -40 to +105 °C [2)] 32 bit LPDDR4 @4266MTs, temperature range Industrial	-25 to +85	4thQ - 2031
SmarCore EHL X6211E 8GB	**0026700251E77A**	58			-25 to +85	4thQ - 2031
SmarCore EHL X6211E 4GB	**0026800251E76A**	1	SMARC 2.**1** short size, Intel EHL X6211E, 4GB LPDDR4, 32GB **eMMC -25°C**[3)], LVDS, DUAL GB ethernet	Intel Atom X6211E dual core 6W 1.2 GHz, 1.5MB L2 cache, Industrial, -40 to +105 °C [2)] 32 bit LPDDR4 @4266MTs, temperature range Industrial	-25 to +85	4thQ - 2031
SmarCore EHL X6211E 4GB	**0026700251E76A**	58			-25 to +85	4thQ - 2031
SmarCore EHL X6413E 8GB	**0026800254E77A**	1	SMARC 2.**1** short size, Intel EHL X6413E, 8GB LPDDR4, 32GB **eMMC -25°C**[3)], LVDS, DUAL GB ethernet	Intel Atom X6413E quad core 9W 1.5 GHz, 1.5MB L2 cache, Industrial, -40 to +105 °C [2)] 32 bit LPDDR4 @4266MTs, temperature range Industrial	-25 to +85	4thQ - 2031
SmarCore EHL X6413E 8GB	**0026700254E77A**	58			-25 to +85	4thQ - 2031
SmarCore EHL X6413E 4GB	**0026800254E76A**	1	SMARC 2.**1** short size, Intel EHL X6413E, 4GB LPDDR4, 32GB **eMMC -25°C**[3)], LVDS, DUAL GB ethernet	Intel Atom X6413E quad core 9W 1.5 GHz, 1.5MB L2 cache, Industrial, -40 to +105 °C [2)] 32 bit LPDDR4 @4266MTs, temperature range Industrial	-25 to +85	4thQ - 2031
SmarCore EHL X6413E 4GB	**0026700254E76A**	58			-25 to +85	4thQ - 2031
SmarCore EHL X6425E 8GB	**0026800256E77A**	1	SMARC 2.**1** short size, Intel EHL X6425E, 8GB LPDDR4, 32GB **eMMC -25°C**[3)], LVDS, DUAL GB ethernet	Intel Atom X6425E quad core 12W 2 GHz, 1.5MB L2 cache, Industrial, -40 to +105 °C [2)] 32 bit LPDDR4 @4266MTs, temperature range Industrial	-25 to +85	4thQ - 2031
SmarCore EHL X6425E 8GB	**0026700256E77A**	58			-25 to +85	4thQ - 2031

Following are provided the ordering information and the description for the module's Starterkit:

Marking Code	Ordering Code	MPQ	Description	Operating temperature range °C (excepted Module)[2)]
Starterkit		1	Multimedia 4K Starterkit SMARC carrier board	-40 to +85

[1)] **Long Term Availability based on INTEL longevity program**

[2)] ***Note: internal junction temperature (Temperature Range TJ Embedded SKUs: -40°C to 105°C - Industrial SKUs: -40°C to 110°C)***

[3)] ***Industrial eMMC option on request***

CHAPTER 3

3.PINOUT AND FEATURES

Section includes :

- **Pinout overview**
- **SMARC supported features**

3.1 KEY FEATURES

SoC:

- Intel Atom X6211E Dual Core @ 1.2 GHz (burst 3.0 GHz) 1.5MB L2 cache, 6W
- Intel Atom X6413E Quad Core @ 1.5 GHz (burst 3.0 GHz) 1.5MB L2 cache, 9W
- Intel Atom X6425E Quad Core @ 1.8 GHz (burst 3.0 GHz) 1.5MB L2 cache, 12W)
- Intel Atom X6212RE Dual Core @ 1.2 GHz, 1.5MB L2 cache, 6W
- Intel Atom X6414RE Quad Core @ 1.5 GHz, 1.5MB L2 cache, 9W
- Intel Atom X6425RE Quad Core @ 1.9 GHz, 1.5MB L2 cache, 12W

Memory:

- Starting from 2GB LPDDR4-4266MTs on board

Storage:

- Starting from 16GB eMMC drive soldered on-board
- SATA Gen3.2
- SD 4bit

Display & Graphics

- Intel® 11th generation (Gen 11) LP graphics controller
- DirectX 12.1 compliant, OpenGL ES 3.1/3.0/2.0/1.1, OpenGL 4.5 supported, OpenCL™ 1.2, Vulkan 1.0 APIs
- Dedicated FIVR for Graphics
- Intel® Virtualization Technology for Directed I/O (VT-d)
- eDP to LVDS Dual channel up to 1920x1080 @ 60Hz via eDP bridge;
- 1 x HDMI up to 4096x2160@60Hz
- 1x DP up to 4096x2160@60Hz
- eDP up to 4096x2160@60Hz

Audio

- I2S Interface

PCIe

- 1 x PCIe 3.0

Ethernet

- 2 x Gb Ethernet interface

I2C

- 3 x I2C

USB

- 2 x USB Host 3.0, 3 x USB Host 2.0
- 1 x USB 2.0

UART

- 4 x High Speed UART

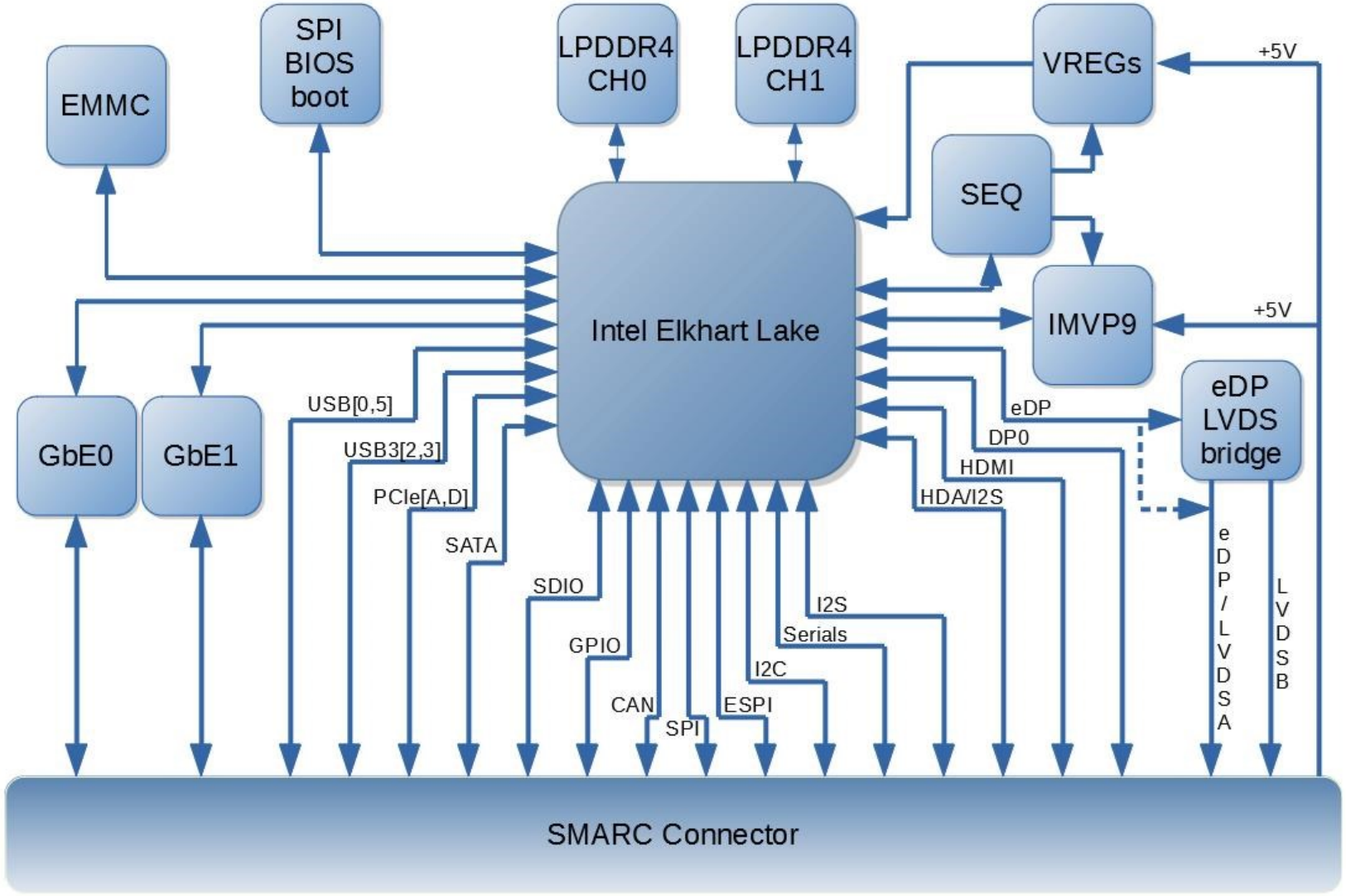
SATA

- 1 x SATA3

SPI

- 2 x SPI interface

3.2 BLOCK DIAGRAM



3.3 MODULE PINOUT COMPARED WITH FULL SET SMARC

There are 314 edge fingers of the SMARC module that mate with a low profile 314 pin 0.5mm pitch right angle connector. The following table lists the module pin assignments for all 314 edge fingers.

P-Pin	SIGNAL	V Rail	GPIO	S-Pin	SIGNAL	V Rail	GPIO
				S1	I2C_CAM1_CK	-	-
P1	SMB_ALERT_1V8#	+1,8V	Y	S2	I2C_CAM1_DAT	-	-
P2	GND	-	-	S3	GND	-	-
P3	CSI1_CK+	-	-	S4	RSVD	-	-
P4	CSI1_CK-	-	-	S5	I2C_CAM0_CK	+1,8V	Y
P5	GBE1_SDP	+3,3V	Y	S6	CAM_MCK	+1,8V	Y
P6	GBE0_SDP	+3,3V	Y	S7	I2C_CAM0_DAT	+1,8V	Y
P7	CSI1_RX0+	-	-	S8	CSI0_CK+	-	-
P8	CSI1_RX0-	-	-	S9	CSI0_CK-	-	-
P9	GND	-	-	S10	GND	-	-
P10	CSI1_RX1+	-	-	S11	CSI0_RX0+	-	-
P11	CSI1_RX1-	-	-	S12	CSI0_RX0-	-	-
P12	GND	-	-	S13	GND	-	-
P13	CSI1_RX2+	-	-	S14	CSI0_RX1+	-	-
P14	CSI1_RX2-	-	-	S15	CSI0_RX1-	-	-
P15	GND	-	-	S16	GND	-	-
P16	CSI1_RX3+	-	-	S17	GBE1_MDI0+	-	N
P17	CSI1_RX3-	-	-	S18	GBE1_MDI0-	-	N
P18	GND	-	-	S19	GBE1_LINK100#	-	
P19	GBE_MDI3-	-	N	S20	GBE1_MDI1+	-	N
P20	GBE_MDI3+	-	N	S21	GBE1_MDI1-	-	N
P21	GBE_LINK100#	+3,3V	N	S22	GBE1_LINK1000#	-	
P22	GBE_LINK1000#	+3,3V	N	S23	GBE1_MDI2+	-	N
P23	GBE_MDI2-	-	N	S24	GBE1_MDI2-	-	N
P24	GBE_MDI2+	-	N	S25	GND	-	
P25	GBE_LINK_ACT#	-	N	S26	GBE1_MDI3+	-	N
P26	GBE_MDI1-	-	N	S27	GBE1_MDI3-	-	N
P27	GBE_MDI1+	-	N	S28	GBE1_CTREF+	-	-
P28	GBE_CTREF	-	-	S29	PCIE_D_TX+	+1,8V	N
P29	GBE_MDI0-	-	N	S30	PCIE_D_TX-	+1,8V	N
P30	GBE_MDI0+	-	N	S31	GBE1_LINK_ACT#	+3,3V	N
P31	SPI0_CS1#	+1,8V	Y	S32	PCIE_D_RX+	+1,8V	N
P32	GND		-	S33	PCIE_D_RX-	+1,8V	N
P33	SDIO_WP	+3,3V	Y	S34	GND	-	
P34	SDIO_CMD	+3,3V	Y	S35	USB4+	USB	N
P35	SDIO_CD#	+3,3V	Y	S36	USB4-	USB	N
P36	SDIO_CK	+3,3V	Y	S37	USB3_VBUS_DET		
P37	SDIO_PWR_EN	+3,3V	Y	S38	AUDIO_MCK	+1,8V	Y
P38	GND		-	S39	I2S0_LRCK	+1,8V	Y
P39	SDIO_D0	+3,3V	Y	S40	I2S0_SDOUT	+1,8V	Y
P40	SDIO_D1	+3,3V	Y	S41	I2S0_SDIN	+1,8V	Y

P-Pin	SIGNAL	V Rail	GPIO	S-Pin	SIGNAL	V Rail	GPIO
P41	SDIO_D2	+3,3V	Y	S42	I2S0_CK	+1,8V	Y
P42	SDIO_D3	+3,3V	Y	S43	ESPI_ALERT0#	+1,8V	Y
P43	SPI0_CS0#	+1,8V	Y	S44	ESPI_ALERT1#	+1,8V	Y
P44	SPI0_CK	+1,8V	Y	S45	RSVD	-	-
P45	SPI0_DIN	+1,8V	Y	S46	RSVD	-	-
P46	SPI0_DO	+1,8V	Y	S47	GND	-	-
P47	GND	-	-	S48	I2C_GP_CK	+1,8V	Y
P48	SATA_TX+		N	S49	I2C_GP_DAT	+1,8V	Y
P49	SATA_TX-		N	S50	HDA_SYNC	+1,8V	Y
P50	GND		-	S51	HDA_SDO	+1,8V	Y
P51	SATA_RX+		N	S52	HDA_SDI	+1,8V	Y
P52	SATA_RX-		N	S53	HDA_CK	+1,8V	Y
P53	GND	-	-	S54	SATA_ACT#	+3,3V	Y
P54	ESPI_CS0#	+1,8V	Y	S55	USB5_EN_OC#	+3,3V	N
P55	ESPI_CS1#	+1,8V	Y	S56	ESPI_IO_2	+1,8V	Y
P56	ESPI_CK	+1,8V	Y	S57	ESPI_IO_3	+1,8V	Y
P57	ESPI_IO_1	+1,8V	Y	S58	ESPI_RESET	+1,8V	Y
P58	ESPI_IO_0	+1,8V	Y	S59	USB5+	USB	N
P59	GND			S60	USB5-	USB	N
P60	USB0+	USB	N	S61	GND		
P61	USB0-	USB	N	S62	USB3_SSTX+	USB	N
P62	USB0_EN_OC#	+3,3V	Y	S63	USB3_SSTX	USB	N
P63	USB0_VBUS_DET	USB	N	S64	GND		
P64	USB0_OTG_ID	USB	N	S65	USB3_SSRX+	USB	N
P65	USB1+	USB	N	S66	USB3_SSRX-	USB	N
P66	USB1-	USB	N	S67	GND		
P67	USB1_EN_OC#	+3,3V	Y	S68	USB3+	USB	N
P68	GND		-	S69	USB3-	USB	N
P69	USB2+	USB	N	S70	GND		
P70	USB2-	USB	N	S71	USB2_SSTX+	USB	N
P71	USB2_EN_OC#	+3,3V	Y	S72	USB2_SSTX	USB	N
P72	RSVD	-	-	S73	GND		
P73	RSVD	-	-	S74	USB2_SSRX+	USB	N
P74	USB3_EN_OC#	+3,3V	Y	S75	USB2_SSRX-	USB	N
P75	PCIE_A_RST#	+3,3V	Y	S76	PCIE_B_RST#	+3,3V	Y
P76	USB4_EN_OC#	+3,3V	N	S77	PCIE_C_RST#	+3,3V	Y
P77	PCIE_B_CLKREQ#	+1,8V	Y	S78	PCIE_C_RX+	+1,8V	N
P78	PCIE_A_CLKREQ#	+1,8V	Y	S79	PCIE_C_RX-	+1,8V	N
P79	GND		-	S80	GND	-	-
P80	PCIE_C_REFCK+	+1,8V	N	S81	PCIE_C_TX+	+1,8V	N
P81	PCIE_C_REFCK-	+1,8V	N	S82	PCIE_C_TX-	+1,8V	N
P82	GND	-	-	S83	GND	-	-
P83	PCIE_A_REFCK+	+1,8V	N	S84	PCIE_B_REFCK+	+1,8V	N
P84	PCIE_A_REFCK-	+1,8V	N	S85	PCIE_B_REFCK-	+1,8V	N
P85	GND	-	-	S86	GND	-	-
P86	PCIE_A_RX+	+1,8V	N	S87	PCIE_B_RX+	+1,8V	N

P-Pin	SIGNAL	V Rail	GPIO	S-Pin	SIGNAL	V Rail	GPIO
P87	PCIE_A_RX-	+1,8V	N	S88	PCIE_B_RX-	+1,8V	N
P88	GND	-	-	S89	GND	-	-
P89	PCIE_A_TX+	+1,8V	N	S90	PCIE_B_TX+	+1,8V	N
P90	PCIE_A_TX-	+1,8V	N	S91	PCIE_B_TX-	+1,8V	N
P91	GND	-	-	S92	GND	-	-
P92	HDMI_D2+ / DP1_LANE0+	-	N	S93	DP0_LANE0+	-	N
P93	HDMI_D2- / DP1_LANE0-	-	N	S94	DP0_LANE0-	-	N
P94	GND	-	-	S95	DP0_AUX_SEL	-	-
P95	HDMI_D1+ / DP1_LANE1+	-	N	S96	DP0_LANE1+	-	N
P96	HDMI_D1- / DP1_LANE1-	-	N	S97	DP0_LANE1-	-	N
P97	GND	-	-	S98	DP0_HPD	-	Y
P98	HDMI_D0+ / DP1_LANE2+	-	N	S99	DP0_LANE2+	-	N
P99	HDMI_D0- / DP1_LANE2-	-	N	S100	DP0_LANE2-	-	N
P100	GND	-	-	S101	GND	-	
P101	HDMI_CK+ / DP1_LANE3+	-	N	S102	DP0_LANE3+	-	N
P102	HDMI_CK- / DP1_LANE3-	-	N	S103	DP0_LANE3-	-	N
P103	GND	-	-	S104	USB3_OTG_ID	-	-
P104	HDMI_HPD / DP1_HPD	+1,8V	Y	S105	DP0_AUX+	+3,3V	N
P105	HDMI_CTRL_CK / DP1_AUX+	+1,8V	Y	S106	DP0_AUX-	+3,3V	N
P106	HDMI_CTRL_DAT / DP1_AUX-	+1,8V	Y	S107	LCD1_BKLT_EN	+1,8V	Y
P107	DP1_AUX_SEL	-	-	S108	LVDS1_CK+	+2,5V	N
P108	GPIO0/CAM0_PWR#	+1,8V	Y	S109	LVDS1_CK-	+2,5V	N
P109	GPIO1/CAM1_PWR#	+1,8V	Y	S110	GND	-	-
P110	GPIO2/CAM0_RST#	+1,8V	Y	S111	LVDS1_0+	+2,5V	N
P111	GPIO3/CAM1_RST#	+1,8V	Y	S112	LVDS1_0-	+2,5V	N
P112	GPIO4/HDA_RST#	+1,8V	Y	S113	eDP1_HPD		
P113	GPIO5/PWM_OUT	+1,8V	Y	S114	LVDS1_1+	+2,5V	N
P114	GPIO6/TACHIN	+1,8V	Y	S115	LVDS1_1-	+2,5V	N
P115	GPIO7	+1,8V	Y	S116	LCD1_VDD_EN		
P116	GPIO8	+1,8V	Y	S117	LVDS1_2+	+2,5V	N
P117	GPIO9	+1,8V	Y	S118	LVDS1_2-	+2,5V	N
P118	GPIO10	+1,8V	Y	S119	GND		
P119	GPIO11	+1,8V	Y	S120	LVDS1_3+	+2,5V	N
P120	GND	-	-	S121	LVDS1_3-	+2,5V	N
P121	I2C_PM_CK	+1,8V	Y	S122	LCD1_BKLT_PWM	+1,8V	Y
P122	I2C_PM_DAT	+1,8V	Y	S123	GPIO13	+1,8V	Y
P123	BOOT_SEL0#	-	-	S124	GND	-	-
P124	BOOT_SEL1#	-	-	S125	LVDS0_0+	+2,5V	N
P125	BOOT_SEL2#	-	-	S126	LVDS0_0-	+2,5V	N
P126	RESET_OUT#	+1,8V	-	S127	LCD_BKLT_EN		N
P127	RESET_IN#	+1,8V	N	S128	LVDS0_1+	+2,5V	N
P128	POWER_BTN#	+1,8V	-	S129	LVDS0_1-	+2,5V	N
P129	SER0_TX	+1,8V	Y	S130	GND	-	-
P130	SER0_RX	+1,8V	Y	S131	LVDS0_2+	+2,5V	N
P131	SER0_RTS#	+1,8V	Y	S132	LVDS0_2-	+2,5V	N

P-Pin	SIGNAL	V Rail	GPIO	S-Pin	SIGNAL	V Rail	GPIO
P132	SER0_CTS#	+1,8V	Y	S133	LCD_VDD_EN		N
P133	GND	-	-	S134	LVDS0_CK+	+2,5V	N
P134	SER1_TX	+1,8V	Y	S135	LVDS0_CK-	+2,5V	N
P135	SER1_RX	+1,8V	Y	S136	GND	-	-
P136	SER2_TX	+1,8V	Y	S137	LVDS0_3+	+2,5V	N
P137	SER2_RX	+1,8V	Y	S138	LVDS0_3-	+2,5V	N
P138	SER2_RTS#	+1,8V	Y	S139	I2C_LCD_CK	+1,8V	N
P139	SER2_CTS#	+1,8V	Y	S140	I2C_LCD_DAT	+1,8V	N
P140	SER3_TX	+1,8V	Y	S141	LCD_BKLT_PWM	+1,8V	N
P141	SER3_RX	+1,8V	Y	S142	GPIO12	+1,8V	Y
P142	GND	-	-	S143	GND	-	-
P143	CAN0_TX	+1,8V	Y	S144	EDP0_HPD	+1,8V	N
P144	CAN0_RX	+1,8V	Y	S145	WDT_TIME_OUT#	+1,8V	Y
P145	CAN1_TX	+1,8V	Y	S146	PCIE_WAKE#	+3,3V	N
P146	CAN1_RX	+1,8V	Y	S147	VDD_RTC	+VDD_RTC	N
P147	VDD_IN	+5Vin	-	S148	LID#	+1,8V	Y
P148	VDD_IN	+5Vin	-	S149	SLEEP#	+1,8V	Y
P149	VDD_IN	+5Vin	-	S150	VIN_PWR_BAD#		N
P150	VDD_IN	+5Vin	-	S151	CHARGING#	+1,8V	Y
P151	VDD_IN	+5Vin	-	S152	CHARGER_PRSNT#	+1,8V	Y
P152	VDD_IN	+5Vin	-	S153	CARRIER_STBY#	+1,8V	N
P153	VDD_IN	+5Vin	-	S154	CARRIER_PWR_ON	+1,8V	N
P154	VDD_IN	+5Vin	-	S155	FORCE_RECOV#	-	-
P155	VDD_IN	+5Vin	-	S156	BATLOW#	+1,8V	Y
P156	VDD_IN	+5Vin	-	S157	TEST#	-	-
				S158	GND	-	-

Note:

The text in grey represents the signals defined in SMARC specification, but not implemented in SMARC EHL.

The text in red represents signals shared with other signals on the connector. Refer to the table below for further details.

Warning: The pad associated to the pins P131 is only an output signal, therefore the "SLEEP#" function is not available on the module (for details see ERRATA doc). Leave this pin unconnected.

3.4 SMARC SUPPORTED FEATURES

The following table summarizes the SMARC features implemented on SMARC EHL compared with the standard specifications. All mandatory features required by the SMARC specification are implemented in the SMARC EHL Module.

Feature	Sub Feature	Mandatory	SMARC EHL implementation	Note
Parallel LCD	24 bit Parallel RGB interface	May	No	
LVDS LCD	18 bit single channel	Should	Yes	
	24 bit single channel – 18 bit compatible	Should	Yes	
	24 bit single channel – standard color map	May	Yes	
	24 bit dual channel – 18 bit compatible	May		
	24 bit dual channel – standard color map	May		
HDMI	HDMI display interface	Should	Yes	
DP on HDMI Pins		May	Yes	
DP++	DisplayPort++	May	Yes	
Camera	CSI0 – 2 lane	Should	Yes	
	CSI1 – 2 lane implementation	May	Yes	
	CSI1 – 4 lane implementation	May	Yes	
SDIO	SDIO (4 bit, for SD cards)	Should	Yes	
SPI	SPI0	Should	Yes	One CS only
	eSPI	Should	Yes	One CS only
I2S	I2S0	Should	Yes	
	I2S1	No	No	
	I2S2	No	No	
	I2S2 – HDA variant	No	No	
I2C	Power Management	Shall	Yes	HW ready
	General Purpose	Shall	Yes	
	Camera	Should	Yes	
	LCD (Parallel or LVDS) Display I/D	Should	Yes	
Serial Ports	SER0 (4 wire)	Shall	Yes	
	SER1 (2 wire)	Shall	Yes	
	SER2 (4 wire)	Should	Yes	
	SER3 (2 wire)	Should	Yes	
CAN Bus	CAN0	May	Yes	
	CAN1	May	Yes	
USB	USB0 - as USB 2.0 Client	Should	Yes	
	USB0 - as USB 2.0 Host	May	Yes	
	USB1 - as USB 2.0 Host	Shall	Yes	

Feature	Sub Feature	Mandatory	SMARC EHL implementation	Note
	USB[2:5] – as USB 2.0 Host	May	Yes	
	USBss[2:3]	May	Yes	
	USB3 - as USB 2.0 Client	May		
PCIe	PCIE_A (x1 Gen 1 Root)	Should	Yes	
	PCIE_B (x1 Gen 1 Root)	May	Yes	
	PCIE_C (x1 Gen 1 Root)	May	Yes	
	PCIE_D (x1 Gen 1 Root)	May	Yes	
	PCIE Target operation	May	No	
	PCIE Gen 2 and Gen 3 operation	May	Yes	
SATA	SATA Gen 1	Should	No	
	SATA Gen 2 operation	May	No	
	SATA Gen 3 operation	May	Yes	
GBE	GBE0	Should	Yes	
	GBE1	May	Yes	
	IEE1588 Trigger Signals (GBE[0:1]_SDP)	May		
Watchdog	WDT Out	Should	Yes	
GPIO	GPIOs – 12x	Shall	Yes	
	GPIO interrupt capability – 12x	Shall	Yes	
	GPIO Camera Support	Shall	Yes	
	GPIO5 PWM capability	Should	Yes	
	GPIO6 Tachin capability	Should	Yes	
Management	System and power management features	Shall	Yes	HW ready
Boot Select		Shall	Yes	See chapter 3.5
Force Recov		Shall	Yes	See Chapter
JTAG	JTAG connector on Module	May	Yes	
RTC		Should	Yes	

CHAPTER 4

4.POWER SUPPLY

Section includes :

- **Power signals**
- **VDDIO Voltage Rail**
- **RTC battery**
- **Control signals and power sequences**
- **Boot modes**
- **Power states**
- **Watchdog**

4.1 POWER SIGNALS

Read carefully the related sections before starting your power stage design. This module needs to be supplied up to +5Vin power. Refer to the table below for the power supply range specification.

Note: the system must provide at least a power of 5A at 5V to allow the start of the module.

	Min	Typ	Max
Voltage range	+4,6V	+5V	+5,25V
Module Current @ 5,0V	-	TBD mA	-

Table

Note: *the measures in the table above are to be considered referred to the module with only the OS running, the use of graphics accelerators or other multimedia applications could be the cause of higher consumption than those indicated.*

The following table shows the module power supply pins numbering. It's strongly recommended to connect all power supply pins in order to avoid damage.

P-Pin	Name	Primary Function Description	S-Pin	Name	Primary Function Description
P2	GND	Power return-Ground reference	S3	GND	Power return-Ground reference
P9	GND	Power return-Ground reference	S10	GND	Power return-Ground reference
P12	GND	Power return-Ground reference	S13	GND	Power return-Ground reference
P15	GND	Power return-Ground reference	S16	GND	Power return-Ground reference
P18	GND	Power return-Ground reference	S25	GND	Power return-Ground reference
P32	GND	Power return-Ground reference	S34	GND	Power return-Ground reference
P38	GND	Power return-Ground reference	S47	GND	Power return-Ground reference
P47	GND	Power return-Ground reference	S61	GND	Power return-Ground reference
P50	GND	Power return-Ground reference	S64	GND	Power return-Ground reference
P53	GND	Power return-Ground reference	S67	GND	Power return-Ground reference
P59	GND	Power return-Ground reference	S70	GND	Power return-Ground reference
P68	GND	Power return-Ground reference	S73	GND	Power return-Ground reference
P79	GND	Power return-Ground reference	S80	GND	Power return-Ground reference
P82	GND	Power return-Ground reference	S83	GND	Power return-Ground reference
P85	GND	Power return-Ground reference	S86	GND	Power return-Ground reference
P88	GND	Power return-Ground reference	S89	GND	Power return-Ground reference
P91	GND	Power return-Ground reference	S92	GND	Power return-Ground reference
P94	GND	Power return-Ground reference	S101	GND	Power return-Ground reference
P97	GND	Power return-Ground reference	S110	GND	Power return-Ground reference
P100	GND	Power return-Ground reference	S119	GND	Power return-Ground reference
P103	GND	Power return-Ground reference	S124	GND	Power return-Ground reference
P120	GND	Power return-Ground reference	S130	GND	Power return-Ground reference
P133	GND	Power return-Ground reference	S136	GND	Power return-Ground reference
P142	GND	Power return-Ground reference	S143	GND	Power return-Ground reference
P147	VDD_IN	Power input voltage-5.0V (5.25V Max)	S158	GND	Power return-Ground reference
P148	VDD_IN	Power input voltage-5.0V (5.25V Max)	-	-	-
P149	VDD_IN	Power input voltage-5.0V (5.25V Max)	-	-	-
P150	VDD_IN	Power input voltage-5.0V (5.25V Max)	-	-	-
P151	VDD_IN	Power input voltage-5.0V (5.25V Max)	-	-	-

P-Pin	Name	Primary Function Description	S-Pin	Name	Primary Function Description
P152	VDD_IN	Power input voltage-5.0V (5.25V Max)	-	-	-
P153	VDD_IN	Power input voltage-5.0V (5.25V Max)	-	-	-
P154	VDD_IN	Power input voltage-5.0V (5.25V Max)	-	-	-
P155	VDD_IN	Power input voltage-5.0V (5.25V Max)	-	-	-
P156	VDD_IN	Power input voltage-5.0V (5.25V Max)	-	-	-

Table 6

Only +5V power support

4.2 VDDIO VOLTAGE RAIL

The module is compliant to SMARC_Hardware_Specification_V2.1.

For details referred to SMARC_Hardware_Specification_V2.1 and Chapter 5 of this document.

4.3 RTC BATTERY

The standard provides a signal to power supply a RTC on module. If not used this pin may be left floating.

Pin	Name	Type / Tolerance	Use
S147	VDD_RTC	Power In	Low current RTC circuit backup power – 3.3V nominal. May be sourced from a Carrier based Lithium cell or Super Cap.
		Power Out (when charging a Super Cap)	The connection with module is obtained by connecting directly the backup battery to the VDD_RTC signal. **Note:** *The module is already designed to manage the charge of backup battery, by a siple 1KOhm series resistor from 3.1V.*

The consumption to feed the RTC when the module is powered off is about 3uA at the nominal battery voltage (3.3 V).

4.4 CONTROL SIGNALS AND POWER SEQUENCES

The module signal CARRIER_PWR_ON exists to ensure that the module is powered before the main body of carrier circuits. The carrier system should not be powered until the module asserts the CARRIER_PWR_ON signal as a high. The hardware of the module should assert CARRIER_PWR_ON when all the module's supplies necessary for module booting are up. The module should continue to assert the signal RESET_OUT# after the release of CARRIER_PWR_ON, for a period enough to allow to the carrier power circuits to come up.

PIN	NAME	CPU PIN NAME	DIRECTION	RAIL	Function Description
S154	CARRIER_PWR_ON	PMC_RSMRST_N	OUT	+1.8V	Carrier power enable from module
S150	VIN_PWR_BAD#	-	IN	+5V	Power bad indication from carrier
S153	CARRIER_STBY#	GP_DSW04_PMC_SLP_S3_N	OUT	+1.8V	Drive low by module during standby
P126	RESET_OUT#	GP_B13_PMC_PLTRST_N	OUT	+1.8V	Reset Output to carrier
P127	RESET_IN#	PMC_SYS_RESET_N	IN	+1.8V	Reset Input from carrier
P128	POWER_BTN#	-	IN	+1.8	Power button Input from carrier
S149	SLEEP#	GP_T10_PSE_HSUART2_RE	IN	+1.8V	Sleep indicator from carrier (NOT available)
S148	LID#	GP_T09_PSE_HSUART2_EN	IN	+1.8V	Lid open/close indication
P122	I2C_PM_DAT	GP_C01_SMB_DATA_PSE_I2C3_SDA_PSE_TGPIO19	BI-DIR	+1.8V	Power management I2C bus data
P121	I2C_PM_CK	GP_C00_SMB_DATA_PSE_I2C3_SDA_PSE_TGPIO18	BI-DIR	+1.8V	Power management I2C bus clock
P1	SMB_ALERT_1V8#	GP_C02_PSE_PWM00_SMB_ALERT_N_PSE_TGPIO29	IN	+1.8V	SM Bus Alert# (interrupt) signal
S151	CHARGING#	GP_T14_PSE_UART2_RTS_N_SIO_UART0_RTS_N_PSE_HSUART2_DE	IN	+1.8V	Charge indicator (low during the charging)
S152	CHARGER_PRSNT#	GP_T15_PSE_UART2_CTS_N_SIO_UART0_CTS_N	IN	+1.8V	Charger present
S157	TEST#	-	IN	+1.8V	Test functions (test point connected)
S155	FORCE_RECOV#	-	IN	+1.8V	Test point connected
S156	BATLOW#	GP_DSW00_PMC_BATLOW_N	IN	+1.8V	Battery low indication

Note:
Refer to SMARC_Hardware_Specification_V2.1 for details

4.5 POWER STATES

The SMARC module supports different power states. In the table below are described the behaviour in the different states.

STATUS	Module Status	Carrier Status	Status Description
Unplugged			No power is applied to the system, except the RTC battery might be available (if used)
Off			System is off, but the carrier board input supply is available
Suspend	The module is in the standby mode all the features are off except the wakeup capable one	All the power rails are available, while the peripherals are stopped via software	System is suspended and waits for a wakeup source (TBT).
Run	CPU is available at 100%	All power rails are on and all the peripherals and CPU features are available	System is running
Reset	All the CPU features are in reset mode, power rails are on	All the peripherals are in reset mode, power rails are on	System is put in reset state by holding RESET_IN# is low

CHAPTER 5

5.INTERFACES

Section includes :

- **Ethernet**
- **USB**
- **USB 3.0**
- **Display & HDMI**
- **LVDS**
- **SATA**
- **SDIO**
- **I2S**
- **HDA/I2C**
- **SPI**
- **Serial**
- **PCIe**
- **Camera i/f**
- **I2C**

It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use GPIO CAPABLE pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.

5.1 ETHERNET

SMARC EHL Module support up to 2 Gigabit Ethernet interfaces. This means that the customer has the possibility to have two autonomous Ethernet with two independent IP address. The following table describes primary GBE signals organization.

PIN	NAME	NOTE
P29	GBE0_MDI0-	Diff100
P30	GBE0_MDI0+	
P26	GBE0_MDI1-	Diff100
P27	GBE0_MDI1+	
P23	GBE0_MDI2-	Diff100
P24	GBE0_MDI2+	
P19	GBE0_MDI3-	Diff100
P20	GBE0_MDI3+	
P21	GBE0_LINK100#	Output OD (12mA) +3,3V Rail
P22	GBE0_LINK1000#	Output OD (12mA) +3,3V Rail
P25	GBE0_LINK_ACT#	Output OD (12mA)
P5	GBE0_SDP	Software Definable Pin

The secondary GBE Ethernet interfaces is available on AFB pins as defined by SMARC specifications.
The following table describes secondary GBE signals organization.

PIN	NAME	NOTE
S18	GBE1_MDI0-	Diff100
S17	GBE1_MDI0+	
S21	GBE1_MDI1-	Diff100
S20	GBE1_MDI1+	
S23	GBE1_MDI2+	Diff100
S24	GBE1_MDI2-	
S27	GBE1_MDI3-	Diff100
S26	GBE1_MDI3+	
S19	GBE1_LINK100#	Output OD (12mA) +3,3V Rail
S22	GBE1_LINK1000#	Output OD (12mA) +3,3V Rail
S31	GBE1_LINK_ACT#	Output OD (12mA)
P6	GBE1_SDP	Software Definable Pin

GBE_LINKx signal can be useful to drive Ethernet led indicators. Each output can drive up to 12 mA.

GBE_LINK100# Signal link for 10/100 Mb speed

GBE_LINK_ACT# Signal act for any speed

GBE_LINK1000# is GPIO controlled by the software

The LED output signals GBE_LINK_ACT#, GBE_LINK100# and GBE_LINK1000# can be connected directly to the LED of the Ethernet jack with suitable serial resistors. There is no need for additional buffering if the current draw does not exceed 10mA. All GBE_LINKx signals act as link and activity indicators. The following table describes GBE_LINKx signal functionality.

SIGNAL	NO LINK	10 Mb LINK/ACT	100 Mb LINK/ACT	1000 MB LINK/ACT
GBE_LINK100#	OFF	ON/BLINK	ON/BLINK	OFF
GBE_LINK1000#	OFF	ON/BLINK	OFF	ON/BLINK
GBE_LINK_ACT#	OFF	ON/BLINK	ON/BLINK	ON/BLINK

5.1.1 LAN IMPLEMENTATION GUIDELINES

The most critical component in the LAN interface is the isolation magnetics connected directly to the MDI differential pair signals of the SMARC module.

It should be carefully qualified for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection and Crosstalk Isolation to pass the IEEE conformance tests and EMI tests.

Even if a SMARC module complies with the basic specifications set forth for IEEE certification, it's still possible that the overall system could fail IEEE testing because of a poor quality or unsuitable external isolation magnetics module and/or improper PCB layout of the carrier board.

Ethernet connectors with integrated magnetics are preferable. If a design with external magnetics is chosen, additional care has to be taken to route the signals between the magnetics and Ethernet connector. If only Fast Ethernet (100Mbit/s) is required, some design cost may be saved by using only 10/100Base-TX magnetics.

The Ethernet MDI signals are analogue differential pair signals which need to be routed carefully.

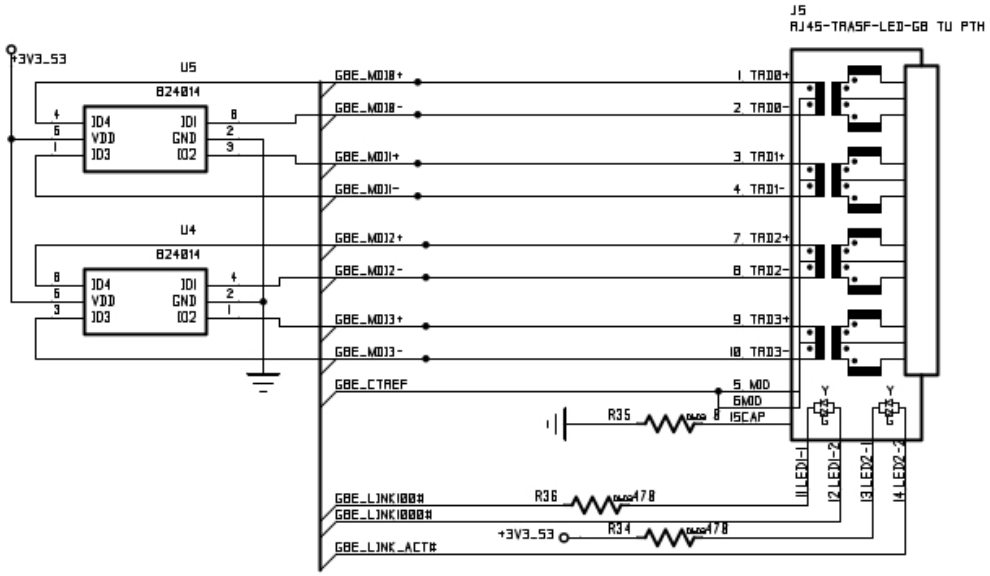
Try to keep the MDI signals as short as possible and keep them away from digital signals. Try to avoid any stubs on these signals.

If discrete magnetics are used instead of a RJ-45 Ethernet jack with integrated magnetics, special care has to be taken to route the signals between the magnetics and the jack. These signals are required to be high voltage isolated from the other signals. It is therefore necessary to place a dedicated ground plane under these signals which has a minimum separation of 2mm from every other signal and plane.

The use of dedicated suppressor is recommended in order to avoid PHY damage by fast high transient voltage peak.

The PHY used in the module is the GPY115CxV1.

The following figure shows a typical GBE connection.



Note:

Refer to the Gbit Ethernet specifications for further details about the board's design and the relative PCB master.

5.2 USB

The USB0 port is available as a USB 2.0.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	NOTE
P60	USB0+	USB2_2_DP	N	USB	Diff90
P61	USB0-	USB2_2_DN	N	USB	
P62	USB0_EN_OC#	GP_E09 / USB2_OC0_N	Y	+3.3V	Enable signal for the bus voltage output and over current input signal for the USB0 interface. Pulled high by module. Carrier can pull low to disable USB. OC connected to USB2_OC0_N_1V8 on CPU.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
P65	USB1+	USB2_3_DP	-	USB	Diff90
P66	USB1-	USB2_3_DN	-	USB	
P67	USB1_EN_OC#	GP_E09 / USB2_OC0_N	-	+3.3V	Enable signal for the bus voltage output and over current input signal for the USB1 interface. Pulled high by module. Carrier can pull low to disable USB. OC connected to USB2_OC0_N_1V8 on CPU.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
P69	USB2+	USB2_0_DP	-	USB	
P70	USB2-	USB2_0_DN	-	USB	
P71	USB2_EN_OC#	GP_T08 / USB2_OC2_N / PSE_TGPIO22	-	+3.3V	Enable signal for the bus voltage output and over current input signal for the USB2 interface. Pulled high by module. Carrier can pull low to disable USB. OC connected to USB2_OC0_N_1V8 on CPU.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
S68	USB3+	USB2_1_DP	-	USB	
S69	USB3-	USB2_1_DN	-	USB	
P74	USB3_EN_OC#	GP_T11 / USB2_OC3_N / PSE_TGPIO06	-	+3.3V	Enable signal for the bus voltage output and over current input signal for the USB3 interface. Pulled high by module. Carrier can pull low to disable USB. OC connected to USB2_OC1_N_1V8 on CPU.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
S35	USB4+	USB2_4_DP	-	USB	
S36	USB4-	USB2_4_DN	-	USB	
P76	USB4_EN_OC#	GP_T06 / PSE_GBE0_AUXTS /USB2_OC1_N	-	+3.3V	Enable signal for the bus voltage output and over current input signal for the USB3 interface. Pulled high by module. Carrier can pull low to disable USB.

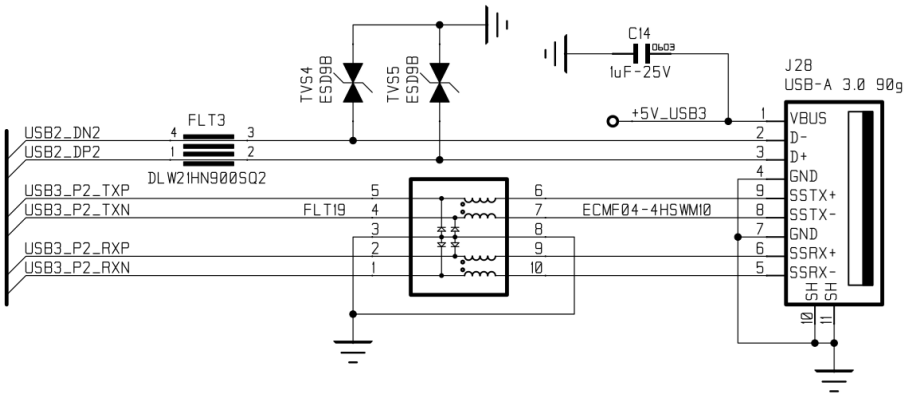
PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
					OC connected to USB2_OC1_N_1V8 on CPU.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
S59	USB5+	USB2_5_DP	-	USB	
S60	USB5-	USB2_5_DN	-	USB	
S55	USB5_EN_OC#	GP_A13/ PSE_GBE1_RGMII_ TXD1	-	+3.3V	Enable signal for the bus voltage output and over current input signal for the USB5 interface. Pulled high by module. Carrier can pull low to disable USB. OC connected to USB2_OC1_N_1V8 on CPU.

* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.

5.2.1 USB 3.0

USB 3.0 interfaces have to be coupled with relative USB 2.0 interfaces. Figure below shows how to couple the interfaces on a standard USB 3.0 type A connector.



PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
S63	USB3_SSTX-	USB3_1_TXN	N	USB SS	To be coupled with USB3, pin S68 and S69.
S62	USB3_SSTX+	USB3_1_TXP	N	USB SS	
S66	USB3_SSRX-	USB3_1_RXN	N	USB SS	
S65	USB3_SSRX+	USB3_1_RXP	N	USB SS	

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	NOTE
S72	USB2_SSTX-	USB3_0_TXN	N	USB SS	To be coupled with USB2, pin P69 and P70.
S71	USB2_SSTX+	USB3_0_TXP	N	USB SS	
S75	USB2_SSRX-	USB3_0_RXN	N	USB SS	
S74	USB2_SSRX+	USB3_0_RXP	N	USB SS	

5.3 DISPLAY PORT - HDMI

SMARC EHL supports Display Port and HDMI. DP0 is configured to support Display Port. DP1 is configured to support HDMI.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	Type	NOTE
S93	DP0_LANE0+	DDI1_TXP0	N	-	Output	
S94	DP0_LANE0-	DDI1_TXN0	N	-	Output	
S95	DP0_AUX_SEL	DP0_AUX_SEL	N	+1.8V	Output	
S96	DP0_LANE1+	DDI1_TXP1	N	-	Output	
S97	DP0_LANE1-	DDI1_TXN1	N	-	Output	
S98	DP0_HDP	GP_E03/DDI1_HPD/PNL_MISC_DDI1/CPU_GP0/PSE_TGPIO15	Y	+1.8V	Input	Active High
S99	DP0_LANE2+	DDI1_TXP2	N	-	Output	
S100	DP0_LANE2-	DDI1_TXN2	N	-	Output	
S102	DP0_LANE3+	DDI1_TXP3	N	-	Output	
S103	DP0_LANE3-	DDI1_TXN3	N	-	Output	
S105	DP0_AUX+	DDI1_AUXP	N	+3.3V	Output	
S106	DP0_AUX-	DDI1_AUXN	N	+3.3V	Output	
P92	HDMI_D2+ / DP1_LANE0+	DDI2_TXP0	N	-	Output	
P93	HDMI_D2- / DP1_LANE0-	DDI2_TXN0	N	-	Output	
P95	HDMI_D1+ / DP1_LANE1+	DDI2_TXP1	N	-	Output	
P96	HDMI_D1- / DP1_LANE1-	DDI2_TXN1	N	-	Output	
P98	HDMI_D0+ / DP1_LANE2+	DDI2_TXP2	N	-	Output	
P99	HDMI_D0- / DP1_LANE2-	DDI2_TXN2	N	-	Output	
P101	HDMI_CK+ / DP1_LANE3+	DDI2_TXP3	N	-	Output	
P102	HDMI_CK- / DP1_LANE3-	DDI2_TXN3	N	-	Output	
P104	HDMI_HPD / DP1_HPD	GP_H20/PSE_PWM07/DDI2_HPD/PSE_TGPIO55	Y	+1.8V	Input	Active High
P105	HDMI_CTRL_CK / DP1_AUX+	GP_H16/PCIE_LNK_DOWN/DDI2_DDC_SCL	Y	+3.3V	Output	
P106	HDMI_CTRL_DAT / DP1_AUX-	GP_H19/DDI2_DDC_SDA/PMC_TGPIO0/PSE_TGPIO20	Y	+3.3V	Output	

* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.

5.4 LVDS

In the SMARCORE module there is only one connection to display with LVDS interface up to Full HD resolution using two channel (LVDS0 and LVDS1). The connection is up to 24 bit data. LVDS signals are generated by an eDP to LVDS bridge.
Optionally the bridge can be removed and the eDP signal can connect to LVDS0 channel.

Following the LVDS interfaces maps and schemes.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	Type	NOTE
S125	LVDS0_0+/eDP0_TX0+	-	-	+2.5V	Output	
S126	LVDS0_0-/eDP0_TX0-	-	-	+2.5V	Output	
S128	LVDS0_1+/eDP0_TX1+	-	-	+2.5V	Output	
S129	LVDS0_1-/eDP0_TX1-	-	-	+2.5V	Output	
S131	LVDS0_2+/eDP0_TX2+	-	-	+2.5V	Output	
S132	LVDS0_2-/eDP0_TX2-	-	-	+2.5V	Output	
S134	LVDS0_CK+/eDP0_AUX+	-	-	+2.5V	Output	
S135	LVDS0_CK-/eDP0_AUX-	-	-	+2.5V	Output	
S137	LVDS0_3+/eDP0_TX3+	-	-	+2.5V	Output	
S138	LVDS0_3-/eDP0_TX3-	-	-	+2.5V	Output	
S133	LCD_VDD_EN	PNL0_BKLTEN	N	+3.3V	Output	
S127	LCD_BKLT_EN	PNL0_VDDEN	N	+1.8V	Output	
S141	LCD_BKLT_PWM	PNL0_BKLTCTL	N	+1.8V	Output	
S111	LVDS1_0+	-	-	+2.5V	Output	
S112	LVDS1_0-	-	-	+2.5V	Output	
S114	LVDS1_1+	-	-	+2.5V	Output	
S115	LVDS1_1-	-	-	+2.5V	Output	
S117	LVDS1_2+	-	-	+2.5V	Output	
S118	LVDS1_2-	-	-	+2.5V	Output	
S108	LVDS1_CK+	-	-	+2.5V	Output	
S109	LVDS1_CK-	-	-	+2.5V	Output	
S120	LVDS1_3+	-	-	+2.5V	Output	
S121	LVDS1_3-	-	-	+2.5V	Output	
S116	LCD1_VDD_EN	GP_D00/PSE_QEPA0/PSE_SPI1_CS0_N/PSE_TGPIO32	Y	+1.8V	Output	
S107	LCD1_BKLT_EN	GP_U07/PSE_QEPA3/PSE_SPI1_MOSI/PSE_TGPIO10	Y	+1.8V	Output	
S122	LCD1_BKLT_PWM	GP_D04/PSE_PWM02/PSE_SPI1_CS1_N/PSE_TGPIO36	Y	+1.8V	Output	
S139	I2C_LCD_CK	GP_HO9/ SIO_I2C4_SDA/ PSE_PWM13	Y	+1.8V	Bi-Dir	LCD display support
S140	I2C_LCD_DAT	GP_HO8/ SIO_I2C4_SDA/ PSE_PWM12	Y	+1.8V	Bi-Dir	LCD display support
S144	EDP0_HPD	GP_E14/DDI0_HPD/PNL_MISC_DDI0/PSE_TGPIO19	Y	+1.8V	Input	PD 220K

* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.

5.4.1 LVDS ROUTING AND PLACEMENT CONSIDERATIONS

The LVDS lines are high-speed signals and as such during the designing must be complied with standards of protection against noise and crosstalk. In this chapter we give some advices about positioning, cabling and routing; for further details, follow the guidelines and the manuals about LVDS bus.
Differential line: as mentioned we are working with fast signals, then to avoid disturbances and reduce noise on the line we suggest routing the channel lines in differential mode, for the same reason also the “channel” on the cable used to connect the board to TFT should be twisted.

Distance: there is no distance recommended between the devices but, always considering the nature of signals and that the driver is the same processor, we suggest to positioning the connector as close as possible to the module, and also to be aware to matching the line of differential pair as best as you can to avoid any kind of delay.
Controlled Impedance: all the signal's pairs must be traced in controlled impedance referred to the GND plane. This should avoid the problems due to reflections on the line. We suggest that the traces for LVDS signals should be closely-coupled and designed for 100Ω differential impedance.

5.5 EDP

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	Type	NOTE
S125	LVDS0_0+/eDP0_TX0+	DDI0_TXP0	-	+2.5V	Output	
S126	LVDS0_0-/eDP0_TX0-	DDI0_TXN0	-	+2.5V	Output	
S128	LVDS0_1+/eDP0_TX1+	DDI0_TXP1	-	+2.5V	Output	
S129	LVDS0_1-/eDP0_TX1-	DDI0_TXN1	-	+2.5V	Output	
S131	LVDS0_2+/eDP0_TX2+	DDI0_TXP2	-	+2.5V	Output	
S132	LVDS0_2-/eDP0_TX2-	DDI0_TXN2	-	+2.5V	Output	
S134	LVDS0_CK+/eDP0_AUX+	DDI0_AUXN	-	+2.5V	Output	
S135	LVDS0_CK-/eDP0_AUX-	DDI0_AUXP	-	+2.5V	Output	
S137	LVDS0_3+/eDP0_TX3+	DDI0_TXP3	-	+2.5V	Output	
S138	LVDS0_3-/eDP0_TX3-	DDI0_TXN3	-	+2.5V	Output	
S133	LCD_VDD_EN	PNL0_BKLTEN	-	+3.3V	Output	
S127	LCD_BKLT_EN	PNL0_VDDEN	-	+1.8V	Output	
S141	LCD_BKLT_PWM	PNL0_BKLTCTL	-	+1.8V	Output	

5.6 SATA

SmarCore EHL implements SATA interface Gen 3.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	Type	NOTE
P48	SATA_TX+	PCIE_8_TXP/SATA_0_TXP/GBE_SGMII_TXP	N	SATA	Output	
P49	SATA_TX-	PCIE_8_TXN/SATA_0_TXN/GBE_SGMII_TXN	N	SATA	Output	
P51	SATA_RX+	PCIE_8_RXP/SATA_0_RXP/GBE_SGMII_RXP	N	SATA	Input	
P52	SATA_RX-	PCIE_8_RXN/SATA_0_RXN/GBE_SGMII_RXN	N	SATA	Input	
S54	SATA_ACT#	GP_E00/SATA_LED_N/SATAXPCIE_0/SATA_0_GP	Y	+3.3V	Output	Active Low SATA activity indicator

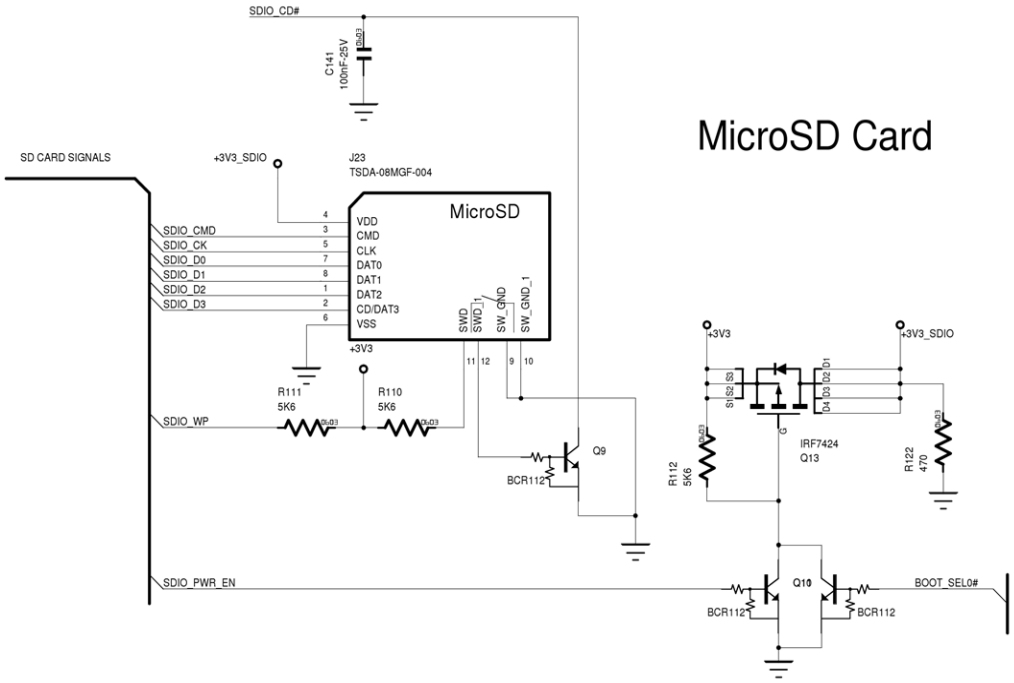
* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.

5.7 SDIO

The module implements SDIO Interface including cards with reduced size or mini cards. The figure below shows how the Micro SD Card connector is connected to the Module in the evaluation board. The SDIO signals of the module's main connector are listed in table below.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
P33	SDIO_WP	GP_G23/SD_SDIO_WP	Y	+3,3V	Input	Write protect
P34	SDIO_CMD	GP_G00/SD_SDIO_CMD	Y	+1,8V	Bi-Dir	Command line
P35	SDIO_CD#	GP_G05/SD_SDIO_CD_N	Y	+1,8V	Input	Card Detect
P36	SDIO_CK	GP_G06/SD_SDIO_CLK	Y	+1,8V	Output	Clock
P37	SDIO_PWR_EN	GP_H17/SD_SDIO_PWR_EN_N	Y	+1,8V	Output	SD power enable
P39	SDIO_D0	GP_G01/SD_SDIO_D0	Y	+1,8V	Bi-Dir	Data
P40	SDIO_D1	GP_G02/SD_SDIO_D1	Y	+1,8V	Bi-Dir	Data
P41	SDIO_D2	GP_G03/SD_SDIO_D2	Y	+1,8V	Bi-Dir	Data
P42	SDIO_D3	GP_G04/SD_SDIO_D3	Y	+1,8V	Bi-Dir	Data

* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.



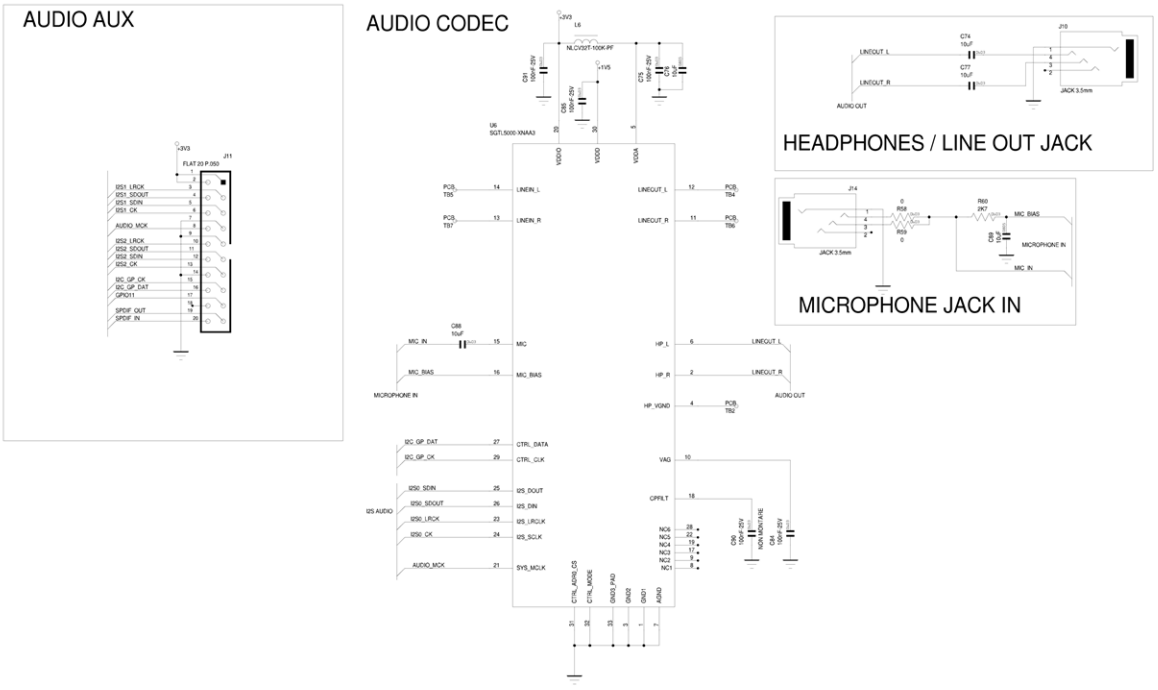
5.8 I2S

I2S, (**Integrated Interchip Sound**), or **IIS**, is an electrical serial bus interface standard used for connecting digital audio devices.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
S38	AUDIO_MCK	GP_D19/AVS_I2S_MCLK1/PSE_TGPIO43	Y	+1.8V	Output	Master clock output to Audio codecs
S39	I2S0_LRCK	GP_G08/AVS_I2S2_SFRM/DMIC_DATA0	Y	+1.8V	Bi-Dir	Left-Right audio sync clock
S40	I2S0_SDOUT	GP_G09/AVS_I2S2_TXD/DMIC_CLK_A1	Y	+1.8V	Output	Digital audio Output (Boot strap)
S41	I2S0_SDIN	GP_G10/AVS_I2S2_RXD/DMIC_DATA1	Y	+1.8V	Input	Digital audio Input
S42	I2S0_CK	GP_G07/AVS_I2S2_SCLK/DMIC_CLK_A0	Y	+1.8V	Bi-Dir	Digital audio clock

* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.

The I2S bus may have a single bidirectional data line or two separate data lines. The bus consists of at least three lines: a serial clock/ bit clock (output from the master), a left right clock (output from the master) that indicates the channel being transmitted and a single data line. It may also include a second data line – and a Master clock signal. A SMARC module can generally be configured as I2S master or slave.
The Engicam's SMARC modules may support up to two independent I2S interfaces both having separate input and output data lines.



5.9 HDA/I2S

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
S50	HDA_SYNC	GP_R01/HDA_SYNC/AVS_I2S0_SFRM/PSE_I2S0_SFRM	Y	+1.8V	Bi-Dir	Left& Right audio synchronization clock / HDA sync, Alternative use: I2S2_LRCK
S51	HDA_SDO	GP_R02/HDA_SDO/AVS_I2S0_TXD/PSE_I2S0_TXD/DMIC_CLK_B0	Y	+1.8V	Output	I2S Digital audio Output / High Definition Audio data out, Alternative use: I2S2_SDOUT
S52	HDA_SDI	GP_R03/HDA_SDI0/AVS_I2S0_RXD/PSE_I2S0_RXD/DMIC_CLK_B1	Y	+1.8V	Input	I2S Digital audio Input / High Definition Audio data in, Alternative use: I2S2_SDI
S53	HDA_CK	GP_R00/HDA_BCLK/AVS_I2S0_SCLK/PSE_I2S0_SCLK	Y	+1.8V	Bi-Dir	I2S Digital audio clock/ High Definition Audio clock, Alternative use: I2S2_CK

* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.

5.10 SPI

In the SMARC modules is available two SPI interfaces, as the SMARC's standard required.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
P43	SPI0_CS0#	GP_D09/PSE_SPI0_CS0_N/SIO_SPI2_CS0_N/PSE_TGPIO10	Y	+1.8V	Output	
P44	SPI0_CK	GP_D10/PSE_SPI0_CLK/SIO_SPI2_CLK/PSE_TGPIO11	Y	+1.8V	Output	
P45	SPI0_DIN	GP_D11/PSE_SPI0_MISO/SIO_SPI2_MISO/PSE_TGPIO12	Y	+1.8V	Input	
P46	SPI0_DO	GP_D12/PSE_SPI0_MOSI/SIO_SPI2_-MOSI/PSE_TGPIO13	Y	+1.8V	Output	
P31	SPI0_CS1#	GP_D15/PSE_PWM03/SIO_SPI2_CS1_N/PSE_SPI0_CS1_N/PSE_TGPIO39	Y	+1.8V	Output	

The following tables describe the Enhanced Configurable SPI signals

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
P54	ESPI_CS0#	GP_G20/ESPI_CS0_N	Y	+1.8V	Output	
P55	ESPI_CS1#	GP_B15/SIO_SPI0_CS0_N/PSE_SPI2_CS0_N/ESPI_CS1_N	Y	+1.8V	Output	
P56	ESPI_CK	GP_G21/ESPI_CLK	Y	+1.8V	Output	
S57	ESPI_IO_3	GP_G18/ESPI_IO3/PMC_SUSACK_N	Y	+1.8V	Bi-Dir	
S56	ESPI_IO_2	GP_G17/ESPI_IO2/PMC_SUSPWRDNACK	Y	+1.8V	Bi-Dir	
P57	ESPI_IO_1	GP_G16/ESPI_IO01	Y	+1.8V	Bi-Dir	
P58	ESPI_IO_0	GP_G15/ESPI_IO0	Y	+1.8V	Bi-Dir	

Note: ESPI SMARC pins can provide ESPI or SPI with mounting option

* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.

5.11 SERIALS

As required into the SMARC specifications the module has up to four asynchronous serial ports interfaces labelled SER0 – SER3.

The signal on the module's UART pins are 1.8V logic level, this cannot be connected directly to a RS232 device like a PC Serial port, the use of a transceivers on the base board is mandatory in order to avoid module damage.

UARTs can be customised via bios. The available options are indicated in brackets.

The following tables describe the specifications of the 4 wires interfaces.

UART0 (PSE_UART4 device 17 function 4, SIO_UART2 device 25 function 2)

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
P129	SER0_TX	GP_C21/PSE_UART4_TXD/SIO_UART2_TXD	Y	+1.8V	Output	
P130	SER0_RX	GP_C20/PSE_UART4_RXD/SIO_UART2_RXD	Y	+1.8V	Input	
P131	SER0_RTS#	GP_C22/PSE_UART4_RTS_N/ISI_SPIM_MOSI/ SIO_UART2_RTS_N	Y	+1.8V	Output	
P132	SER0_CTS#	GP_C23/PSE_UART4_CTS_N/ISI_SPIM_MOSI/ SIO_UART2_CTS_N	Y	+1.8V	Input	

UART2 (PSE_UART0 device 17 function 0, SIO_UART1 device 30 function 1)

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
P136	SER2_TX	GP_C13/PSE_UART0_TXD/SIO_UART1_TXD	Y	+1.8V	Output	
P137	SER2_RX	GP_C12/PSE_UART0_RXD/SIO_UART1_RXD	Y	+1.8V	Input	
P138	SER2_RTS#	GP_C14/PSE_UART0_RTS_N/PSE_HSUAT0_DE/SIO_UART1_RTS_N	Y	+1.8V	Output	
P139	SER2_CTS#	GP_C15/PSE_UART0_CTS_N/SIO_UART1_CTS_N	Y	+1.8V	Input	

The following tables describe the specifications of the 2 wires interfaces

UART1 (PSE_UART2 device 17 function2, SIO_UART0 device 30 function 0)

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
P134	SER1_TX	GP_T13/PSE_UART2_TXD/SIO_UART0_TXD	Y	+1.8V	Output	
P135	SER1_RX	GP_T12/PSE_UART2_TXD/SIO_UART0_TXD	Y	+1.8V	Input	

UART3 (PSE_UART3 device 17 function 3)

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
P140	SER3_TX	GP_C17/GBE_MDC/PSE_UART3_TXD/SIO_I2C0_SCL	Y	+1.8V	Output	
P141	SER3_RX	GP_C16/GBE_MDIO/PSE_UART3_RXD/SIO_I2C0_SDA	Y	+1.8V	Input	

* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.

5.12 PCIE

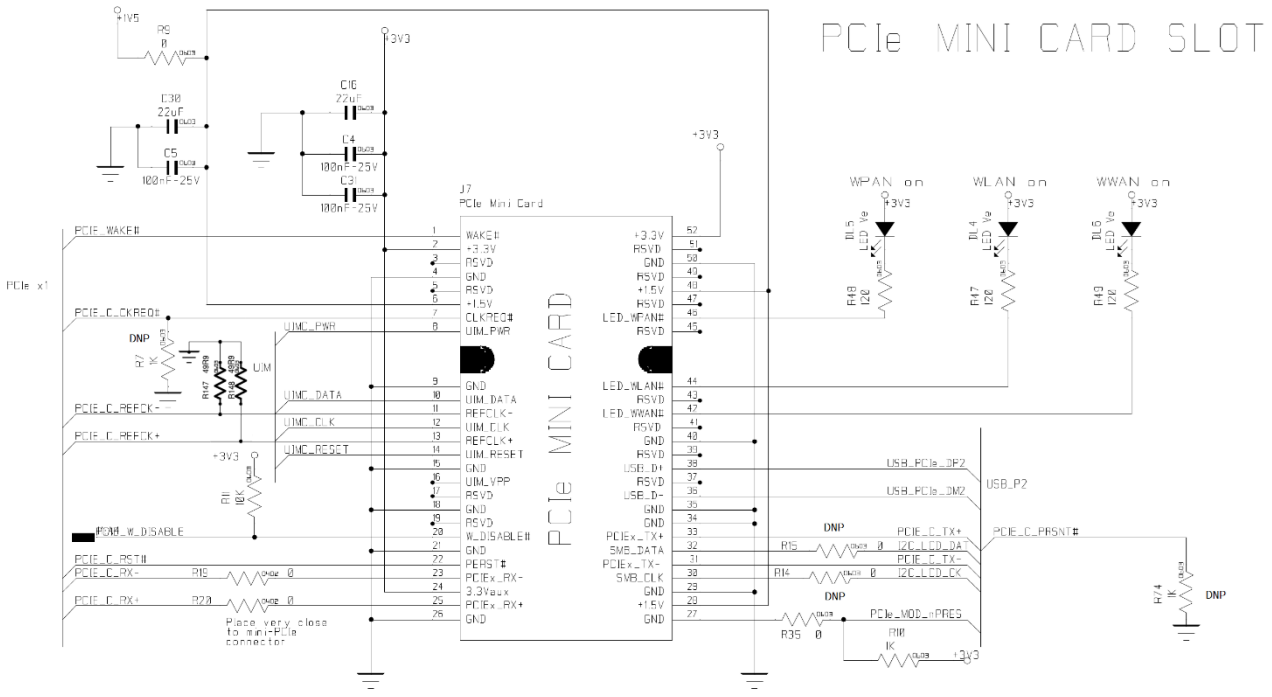
SMARC EHL can support up to 4 external devices on PCIe lines. Possible configurations are:

SMARC PCIe Lane	Possible Link Configuration			
PCIe A	x1	x1	x2	x4
PCIe B	x1	x1		
PCIe C	x1	x2	x2	
PCIe D	x1			

Compliant with the specification the module implements the PCIe Link A port.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
P75	PCIE_A_RST#	GP_D01/PSE_QEPB0/PSE_SPI1_CLK/PSE_TGPIO33	Y	+3.3V	Output	PCIe reset, required PU min 47kΩ
P83	PCIE_A_REFCK+	PCIE_CLK0_DP	-		Output	Differential PCIe reference clock
P84	PCIE_A_REFCK-	PCIE_CLK0_DN	-		Output	Differential PCIe reference clock
P86	PCIE_A_RX+	PCIE_0_RXP/USB3_2_RXP	-		Input	Differential PCIe receive data
P87	PCIE_A_RX-	PCIE_0_RXN/USB3_2_RXN	-		Input	Differential PCIe receive data
P89	PCIE_A_TX+	PCIE_0_TXP/USB3_2_TXP	-		Output	Differential PCIe transmit data
P90	PCIE_A_TX-	PCIE_0_TXN/USB3_2_TXN	-		Output	Differential PCIe transmit data
S146	PCIE_WAKE#	PCM_WAKE_N		+3.3V	Input	PCIe wake up interrupt

* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.



Termination is required on the differential clock lines. Connect two 49.9 Ω resistors, one between REFCLK and GND, the other between REFCLK+ and GND. Alternately, Connect a 100 Ω resistor between REFCLK- and REFCLK+, as close as possible to the receiver device (connector).

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
S76	PCIE_B_RST#	GP_D03/PSE_PWM06/PSE_SPI1_MOSI/PSE_TGPIO35	-	+3.3V	Output	PCIe reset, required PU min 47kΩ
S84	PCIE_B_REFCK+	PCIE_CLK1_DP	-		Output	Differential PCIe reference clock
S85	PCIE_B_REFCK-	PCIE_CLK1_DN	-		Output	Differential PCIe reference clock
S87	PCIE_B_RX+	PCIE_1_RXP/USB3_3_RXP	-		Input	Differential PCIe receive data
S88	PCIE_B_RX-	PCIE_1_RXN/USB3_3_RXN	-		Input	Differential PCIe receive data
S90	PCIE_B_TX+	PCIE_1_TXP/USB3_3_TXP	-		Output	Differential PCIe transmit data
S91	PCIE_B_TX-	PCIE_1_TXN/USB3_3_TXN	-		Output	Differential PCIe transmit data

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
S77	PCIE_C_RST#	GP_D02/PSE_QEPI0/PSE_SPI1_MISO/PSE_TGPIO34	-	+3.3V	Output	PCIe reset, required PU min 47kΩ
P80	PCIE_C_REFCK+	PCIE_CLK2_DP	-		Output	Differential PCIe reference clock
P81	PCIE_C_REFCK-	PCIE_CLK2_DN	-		Output	Differential PCIe reference clock
S78	PCIE_C_RX+	PCIE_2_RXP	-		Input	Differential PCIe receive data
S79	PCIE_C_RX-	PCIE_2_RXN	-		Input	Differential PCIe receive data
S81	PCIE_C_TX+	PCIE_2_TXP	-		Output	Differential PCIe transmit data
S82	PCIE_C_TX-	PCIE_2_TXN	-		Output	Differential PCIe transmit data

PCIe channel D has not got dedicated REFCK and RST signals so it can be used coupled (in x2 or in x4) with other PCIe lines o r in single mode but generating the clock signal on carrier board.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	NOTE
S32	PCIE_D_RX+	PCIE_3_RXP	-		Input	Differential PCIe receive data
S33	PCIE_D_RX-	PCIE_3_RXN	-		Input	Differential PCIe receive data
S29	PCIE_D_TX+	PCIE_3_TXP	-		Output	Differential PCIe transmit data
S30	PCIE_D_TX-	PCIE_3_TXN	-		Output	Differential PCIe transmit data

5.13 GPIO

The following pins, compliant with SMARC specifications, are allocated as general purpose IO, they have all the bidirectional capability but also a preferred direction. These GPIOs can generate directly a CPU interrupt (IRQ) with a specific number. Table below shows the GPIOs and the IRQ numbers.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE	RAIL	TYPE	COMMUNITY	OFFSET
P108	GPIO0/CAM0_PWR#	GP_H04/SIO_I2C2_SDA/PSE_PWM08/PSE_TGPIO10	Y	+1.8V	Bi-Dir/Output	1	20
P109	GPIO1/CAM1_PWR#	GP_H05/SIO_I2C2_SCL/PSE_PWM09/PSE_TGPIO11	Y	+1.8V	Bi-Dir/Output	1	21
P110	GPIO2/CAM0_RST#	GP_T01/ PSE_QEPB2/ SIO_I2C6_SCL/ PSE_TGPIO09	Y	+1.8V	Bi-Dir/Output	0	27
P111	GPIO3/CAM1_RST#	GP_T00/ PSE_QEPA2/ SIO_I2C6_SDA/ PSE_TGPIO08	Y	+1.8V	Bi-Dir/Output	0	26
P112	GPIO4/HDA_RST#	GP_R04/HDA_RST_N/DMIC_CLK_A1	Y	+1.8V	Bi-Dir/Output	5	4
P113	GPIO5/PWM_OUT	GP_H11/PCIE_CLKREQ5_N/ PSE_PWM15	Y	+1.8V	Bi-Dir/Output	1	27
P114	GPIO6/TACHIN	GP_T03/SIO_I2C7_SCL/PSE_TGPIO06	Y	+1.8V	Bi-Dir/Input	0	29
P115	GPIO7	GP_C09/PSE_HSUART0_EN	Y	+1.8V	Bi-Dir	4	9
P116	GPIO8	GP_C11/PSE_HSUART0_RE	Y	+1.8V	Bi-Dir	4	11
P117	GPIO9	GP_H13/PSE_UART1_TXD/ M2_SKT2_CFG1/ PSE_TGPIO52	Y	+1.8V	Bi-Dir	1	29
P118	GPIO10	GP_H12/PSE_UART1_TXD/ M2_SKT2_CFG0/ PSE_TGPIO51	Y	+1.8V	Bi-Dir	1	28
P119	GPIO11	GP_T02/PSE_QEPI2/SIO_I2C7_SDA/PSE_TGPIO07	Y	+1.8V	Bi-Dir	0	28

5.14 I2C

An I2C interface is needed for MOST bus support. The Module I2C_GP port may be used.

PIN	NAME	CPU PIN NAME	GPIO CAPABLE *	RAIL	TYPE	NOTE
S48	I2C_GP_CK	GP_H07/ SIO_I2C3_SCL/ PSE_I2C5_SCL/ PSE_PWM11	Y	+1.8V	Bi-Dir	I2C Bus Clock
S49	I2C_GP_DAT	GP_H06/ SIO_I2C3_SDA/ PSE_I2C5_SDA/ PSE_PWM10	Y	+1.8V	Bi-Dir	I2C Bus Data

* It is strongly recommended to use the GPIO in Chapter 5.13 to be compliant with the SMARC standard. If you decide to use those pins as GPIO, you will definitely lose the indicated feature. A customised BIOS modification will be required.

5.14.1 I2C SLAVE ADDRESS

(pin S139, S140) I^2C4 = eDP to LVDS bridge (0xC0h)
(pin P1, P121, P122) I^2C3 = SM Bus (0x44)

CHAPTER 7

7.PRODUCT COMPLIANCE

In order to respect own internal policy regarding the environmental regulations and safety laws, Engicam in this chapter confirms the compliant, when applicable, of its own products to the normatives ROHS and REACH and to the recognized hazards.
No hazard to report!

CHAPTER 8

8.ENGICAM INFORMATION

8.1 DISCLAIMER

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Engicam explicitly reserves the rights to change or add to the contents of this manual or parts of it without special notification. All operating parameters must be validated for each customer application by customer's technical experts.

8.2 SUPPORT

We offer an on-line support to allow the customer to stay updated on the development of software release and on the enhancement of the documentation.

ENGICAM Product Experts are available to answer questions via email:

support@engicam.com

8.3 CONTACT INFORMATION

Engicam s.r.l.
Via dei Pratoni, 16
50018 Scandicci (Florence) Italy
Tel. +39 055 731 1387
Tel. +39 055 72 06 08
info@engicam.com