MICROGEA MX6 ULL HW MANUAL
GETTING STARTED MANUAL

***** Revision History *****

DATE	REVISION	CHANGE DESCRIPTION
29/11/2017	1.0.0	Release
21/02/2018	1.0.1	Proofread & correct grammar & added connector code for the Carrier board's interface
05/04/2018	1.0.2	Added connector information, moved chapter 7 to the adapter application notes
17/07/2018	1.0.3	Added Resistive Touch information. Updated sleep mode current consumption
18/07/2018	1.0.4	Updated ordering Information table
17/09/2018	1.0.5	Added in-rush current requirements during start-up
24/10/2018	1.0.6	Updated ordering code, update mechanical information, updated LCD and touch connections chapter
01/03/2019	1.0.7	Added reset chapter, general enhancements
04/03/2019	1.0.8	Added current consumption on module's RTC
08/01/2020	1.0.9	Updated Ordering numbers for NAND replacement (PCN_1910-1)
17/03/2020	1.1.0	Updated modules availability based on NXP longevity program; updated LCD specs
20/04/2020	1.1.1	Added codes on Ordering numbers table
21/04/2020	1.1.2	Corrected Ordering numbers table
06/05/2020	1.1.3	Added info on peripherals available on modules equipped with MCIMX6Y1
09/06/2020	1.1.4	Added GPIO and voltage ref info into the pinout table
08/10/2020	1.1.5	Added link to boot config pins chapter, added pin for mux of the UART5_CTS signal
02/11/2020	1.1.6	Added the second Ethernet peripheral's mapping and the considerations of the use of signals ENET_MDC and ENET_MDIO as GPIO
05/02/2021	1.1.7	Ordering code update
24/08/2021	1.1.8	Replaced new Logo on header
05/12/2022	1.1.9	Added information on Phy Ethernet
08/02/2023	1.2.0	Ordering code update
20/04/2023	1.2.1	Ordering code update
02/04/2024	1.2.2	Added information on Phy Ethernet, updated ordering information
05/12/2024	1.2.3	Updated reset pin chapter

TABLE OF CONTENTS

CHAPTER 1

1. INTRODUCTION

This Chapter gives background information on this document.

Section includes :

- ✓ **General Overview**
- ✓ **Acronyms and Abbreviations Used**
- ✓ **Document and Standard References**

1.1 INTRODUCTION

This document is created to guide users to design MicroGEA compliant carrier board. It will focus only on the interfaces in MicroGEA pinouts and related peripherals.

This document helps walk hardware designers through the various stages of designing a carrier board on this platform. Using this document, hardware designers can efficiently locate the resources they need at every step in the board design flow.

All examples of this document are based on MicroGEA carrier and test board. This document also provides a collection of useful documentation, application reports, and design recommendations.

1.2 ACRONYMS AND ABBREVIATIONS USED

ABBREVIATION	EXPLANATION
ADC	Analogue to Digital Converter
CAN	Controller Area Network, a bus that is manly used in automotive and industrial environment
CPU	Central Processor Unit
DAC	Digital to Analogue Converter
EMI	Electromagnetic Interference, high frequency disturbances
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic- sensitive devices
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured being an input or output
HDMI	High-Definition Multimedia Interface, combines audio and video signal
OTG	USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface
PCB	Printed Circuit Board
PD	Pull Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, integrated circuit that manages amongst others the power sequence of a system
PU	Pull Up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, colour channels in common display interfaces
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SPI	Serial Peripheral Interface Bus, synchronous four wire full duplex bus for peripherals
USB	Universal Serial Bus, serial interface for internal and external peripherals

1.3 DOCUMENT AND STANDARD REFERENCES

1.3.1 EXTERNAL INDUSTRY STANDARD DOCUMENTS

- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- USB Specifications (www.usb.org).

1.3.2 NXP DOCUMENTS

- IMX6ULLRM
- IMX6ULLIEC
- IMX6ULLCEC
- IMX6ULLEVKHUG
- IMX6ULLHDG
- L4.1.15_2.0.0-LINUX-DOCS

2. MECHANICAL DATA

This Chapter gives information about PCB and module's dimensions.

Section includes :

- ✓ **Mechanical data**
- ✓ **Assembly Top view**
- ✓ **Assembly Bottom view**
- ✓ **Interface Connectors**

2.1 MECHANICAL DATA

2.2 ASSEMBLY TOP VIEW

In the Figure below is shown top view assembly plan.

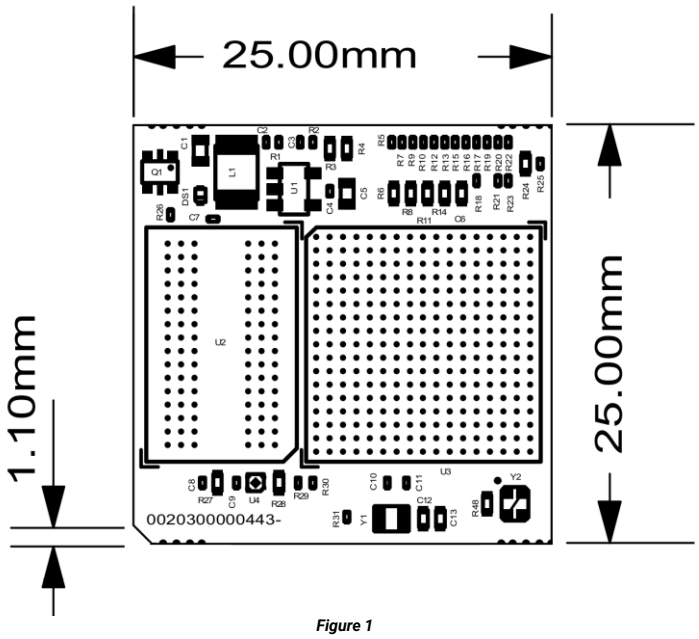


Figure 1

2.3 ASSEMBLY BOTTOM VIEW

The Figure below shows the bottom view assembly plan.

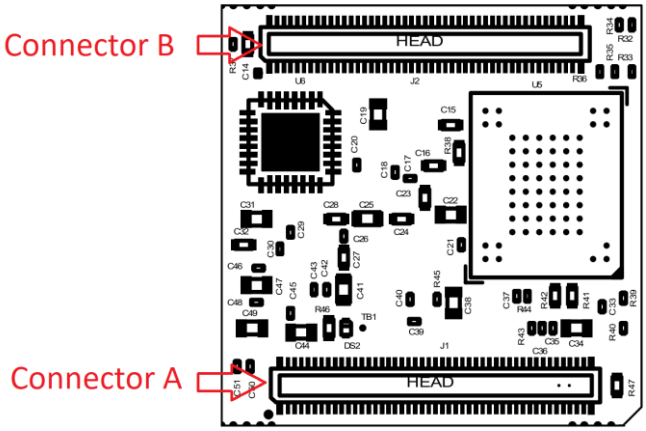


Figure 2

Note: *the connectors interface on module are HRS* code **DF40C-90DP** *that mates with HRS* code **DF40C-90DS (for further details refer to *Chapter 2.4*)**

2.4 INTERFACE CONNECTORS

The following information report the connectors, referred to the series DF40 (HRS) compliant with the MicroGEA SOM interface

CARRIER CONNECTORS

■Product Number Structure (Standard, non-shielded type)

Refer to this page when determining product specifications by model types. Please place orders with part numbers listed in this catalog. The characteristics and specifications of the product described in this catalog are reference values. Please make sure to check the latest delivery specifications at the time of product use.

●Receptacle

DF40	#	–	(**)	–	*	DS	–	0.4	V	(**)
❶	❷		❸		❹	❺		❻	❼	❽

❶ Series Name: DF40

❷ Style
C: Without reinforcing metal fitting
HC: Without reinforcing metal fitting
(The H denotes a stacking height 2.5 mm or above)

❸ Stacking height

Display	Stacking height
None	1.5mm
2.0	2.0mm
2.5	2.5mm
3.0	3.0mm
3.5	3.5mm
4.0	4.0mm

❹ No. of Contacts

❺ Connector Type
DS: Double row receptacle

❻ Contact Pitch:0.4mm

❼ Mating direction Shape V: Vertical SMT

❽ Packaging Type
(51) Embossed tape packaging

Note: for information on the connectors' positioning on carrier board, refer to Chapter 5.1.4

CHAPTER 3

3. ORDERING INFORMATION AND FEATURES

This Chapter gives the ordering information and technical specifications of the modules.

Section includes：

- ✓ **MicroGEAMX6ULL Ordering code**
- ✓ **CPU & memory specifications**
- ✓ **Operating temperature range**

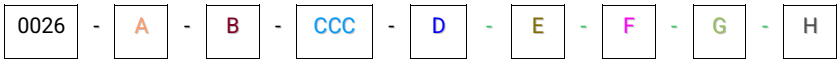
3.1 ORDERING INFORMATION

Following we provide the ordering information and the description for the Basic technical specifications modules:

Part name	Ordering Code	MPQ	Description	CPU & Memory specifications	CPU junction temperature range °C	Operating temperature range °C (excepted CPU)	Module available at least until [1]
MicroGEA MX6ULL 512MB LCD	**0026800082I13B**	1	uGEA i.MX6ULL, 512MB DDR3L, 512MB NAND, Single Ethernet, Industrial	i.MX6ULL Industrial Temperature MCIMX6Y2, 800MHz, 512MB NAND 16 bit Memory temperature range industrial	-40 to +105	-40 to +85	4th Q -2031
MicroGEA MX6ULL 512MB LCD	**0026700082I13B**	58			-40 to +105	-40 to +85	4th Q -2031
MicroGEA MX6ULL 256MB LCD	**0026800082I12B**	1	uGEA i.MX6ULL,256MB DDR3L, 512MB NAND, Single Ethernet, Industrial	i.MX6ULL Industrial Temperature MCIMX6Y2, 800MHz, 512MB NAND 16 bit Memory temperature range industrial	-40 to +105	-40 to +85	4th Q -2031
MicroGEA MX6ULL 256MB LCD	**0026700082I12B**	58			-40 to +105	-40 to +85	4th Q -2031
MicroGEA MX6ULL 128MB NO-LCD	**0026810082I11B**	1	uGEA i.MX6ULL,128MB DDR3L, 512MB NAND, Single Ethernet, Industrial	i.MX6ULL Industrial Temperature MCIMX6Y1, 528MHz, 512MB NAND 16 bit Memory temperature range industrial, NO-LCD	-40 to +105	-40 to +85	4th Q -2031
MicroGEA MX6ULL 128MB NO-LCD	**0026710082I11B**	58			-40 to +105	-40 to +85	4th Q -2031
MicroGEA MX6ULL EPD	**0026800087C010**	-	uGEA i.MX6ULL,128MB DDR3L, 256MB NAND, Single Ethernet, Consumer	i.MX6ULL Consumer Temperature MCIMX6Y7, 900MHz, 256MB NAND 16 bit Memory temperature range industrial	0 to +95	-40 to +85	4th Q -2031
MicroGEA MX6ULL EPD	**0026700087C010**	-			0 to +95	-40 to +85	4th Q -2031
MicroGEA MX6ULL 1GB [2] –LCD	**0026800082I14B**	1	uGEA i.MX6ULL,1 GB DDR3L, 512MB NAND, Single Ethernet, Industrial	i.MX6ULL Industrial Temperature MCIMX6Y2, 800 MHz, 512MB NAND Single Ethernet	-40 to +105	-40 to +85	4th Q -2031
MicroGEA MX6ULL 1GB [2] –LCD	**0026700082I14B**	58			-40 to +105	-40 to +85	4th Q -2031

Table 1

1) **Long Term Availability based on NXP longevity program**
2) **Not in stock, please ask**



H	Reserved

MPQ	A
58	7
1	8

G	RAM SIZE
0	-
1	128MB
-	-
3	512MB
4	1GB
-	-

OPTION AVAILABLE	B
No option	0
No LCD	1
-	-

F	SPECIFICATIONNON VOLATILE MEMORY
0	256MB SLC NAND
1	512MB SLC NAND
-	-
-	-
-	-

SOM TYPE	CCC
MicroGEA	008
-	-
-	-
-	-
-	-

E	TEMPERATURE QUALIFIER
C	Consumer
-	-
I	Industrial-
-	-

CPU TYPE RELATED TO SOM	D
MCIMX6Y2	2
MCIMX6Y7	7
-	-
-	-

Ordering Code nomenclature

In the following table is summarized the key feature differences of processor of i.MX 6ULL series.

Peripherals available on module with CPU	MCIMX6Y1	MCIMX6Y2	MCIMX6Y7
LCD	No	Yes	Yes
CSI	No	Yes	Yes
EPD	No	No	Yes
CAN	1	Up to 2	No
Ethernet	1	Up to 2	Up to 2
USB OTG	Yes	Yes	Yes
UART	Yes	Yes	Yes
I2S	Yes	Yes	Yes
PWM	Yes	Yes	Yes
I2C	Yes	Yes	Yes
SPI	Yes	Yes	Yes

For further details see NXP's documentation

CHAPTER 4

4. PINOUT

This Chapter gives the pinout information.

Section includes：

- ✓ **Pinout overview**
- ✓ **i.MX Pad spacifications**
- ✓ **Electrical specification**

4.1 MODULE PINOUT

The module's interface is achieved by 2 connector HRS code DF40C-90DP that mates with HRS code DF40C-90DS on the carrier board, or compatible (for further details refer to Chapter 2.4)

A -CONNECTOR J1

ODD	NAME	PAD on i.MX	DESCRIPTION	GPIO	Voltage	EVEN	NAME	PAD on i.MX	DESCRIPTION	GPIO	Voltage
1	GND	-	Ground	N		2	USB_OTG_ID	UART3_TX_DATA	USB on the go interface	Y	+3,3V
3	OSC_32KHZ_OUT	GPIO1_IO03	Spare (wiFi) CKL ref	Y	+3,3V	4	USB_OTG_DN	USB_OTG1_DN	USB on the go interface	-	-
5	NC	-	Not Connect	-	-	6	USB_OTG_DP	USB_OTG1_DP	USB on the go interface	-	-
7	UART4_TXD	UART4_TX_DATA	UART TX OUT	Y	+3,3V	8	USB_H1_DN	USB_OTG2_DN	USB on the go interface	-	-
9	UART4_RXD	UART4_RX_DATA	UART RX IN	Y	+3,3V	10	USB_H1_DP	USB_OTG2_DP	USB on the go interface	-	-
11	GND	-	Ground	N	-	12	USB_OTG_VBUS	USB_OTG1_VBUS	+5V power supply for USB OTG engine	N	-
13	NC	-	Not Connect	-	-	14	USB_H1_VBUS	USB_OTG2_VBUS	+5V power supply for USB HOST engine	N	-
15	NC	-	Not Connect	-	-	16	GND	-	Ground	N	-
17	NC	-	Not Connect	-	-	18	+Vcoin	-	CPU RTC backup voltage	-	-
19	+3V3	-	Main power supply	N	-	20	+3V3	-	Main power supply	N	-
21	+3V3	-	Main power supply	N	-	22	+3V3	-	Main power supply	N	-
23	NC	-	Not Connect		-	24	NC	-	Not Connect		-
25	GPIO1_IO09	GPIO1_IO09	General GPIO	Y	+3,3V	26	UART1_RXD	UART1_RX_DATA	UART RX IN	Y	+3,3V
27	GPIO1_IO04	GPIO1_IO04	General GPIO	Y	+3,3V	28	UART1_TXD	UART1_TX_DATA	UART TX OUT	Y	+3,3V
29	GPIO5_2	SNVS_TAMPER2	General GPIO	Y	+3,3V	30	I2C2_SCL	GPIO1_IO00	I2C signal (pull-up needed on carrier)	Y	+3,3V
31	GPIO1_IO10	JATG_MOD	General GPIO	Y	+3,3V	32	GND	-	Ground		
33	GPIO1_IO05	GPIO1_IO05	General GPIO	Y	+3,3V	34	GPIO1_IO02	GPIO1_IO02	General GPIO	Y	+3,3V
35	GPIO1_IO08	GPIO1_IO08	General GPIO	Y	+3,3V	36	GPIO1_25	UART3_RX_DATA	General GPIO	Y	+3,3V
37	GPIO5_0	SNVS_TAMPER0	General GPIO	Y	+3,3V	38	GPIO5_5	SNVS_TAMPER5	General GPIO	Y	+3,3V
39	GPIO5_3	SNVS_TAMPER3	General GPIO	Y	+3,3V	40	GPIO5_4	SNVS_TAMPER4	General GPIO	Y	+3,3V
41	GPIO5_6	SNVS_TAMPER6	General GPIO	Y	+3,3V	42	GPIO5_1	SNVS_TAMPER1	General GPIO	Y	+3,3V
43	GPIO5_7	SNVS_TAMPER7	General GPIO	Y	+3,3V	44	GND	-	Ground	N	-
45	GND	-	Ground	N	-	46	NC	-	Not Connect	-	-
47	BOOT_MODE0	BOOT_MODE0	Boot mode selection	N	-	48	I2C2_SDA	GPIO1_IO01	I2C signal (pull-up needed on carrier)	Y	+3,3V
49	BOOT_MODE1	BOOT_MODE1	Boot mode selection	N	-	50	NC	-	Not Connect	-	-
51	NC	-	Not Connect	-	-	52	LCD_BKL_PWM	ENET1_RX_ER	LCD backlight control	Y	+3,3V

ODD	NAME	PAD on i.MX	DESCRIPTION	GPIO	Voltage	EVEN	NAME	PAD on i.MX	DESCRIPTION	GPIO	Voltage
53	I2S_DIN	JTAG_TCK	I2S Data In	Y	+3,3V	54	NC	-	Not Connect	-	-
55	I2S_DOUT	JTAG_TRST	I2S Data Out	Y	+3,3V	56	NC	-	Not Connect	-	-
57	I2S_LRCLK	JTAG_TDO	I2S RCLK	Y	+3,3V	58	NC	-	Not Connect	-	-
59	I2S_SCLK	JTAG_TDI	I2S SCLK	Y	+3,3V	60	NC	-	Not Connect	-	-
61	GND	-	Ground	N	-	62	NC	-	Not Connect	-	-
63	GND	-	Ground	N	-	64	NC	-	Not Connect	-	-
65	UART2_RXD	UART2_RX_DATA	UART RX IN	Y	+3,3V	66	NC	-	Not Connect	-	-
67	UART2_TXD	UART2_TX_DATA	UART TX OUT	Y	+3,3V	68	GND	-	Ground	N	-
69	UART2_RTS	UART2_RTS	UART RTS signal IN	Y	+3,3V	70	NC	-	Not Connect	-	-
71	UART2_CTS	UART2_CTS	UART CTS signal OUT	Y	+3,3V	72	GND	-	Ground	N	-
73	UART5_RXD	UART5_RX_DATA	UART RX IN	Y	+3,3V	74	NC	-	Not Connect	-	-
75	UART5_TXD	UART5_TX_DATA	UART TX OUT	Y	+3,3V	76	NC	-	Not Connect	-	-
77	NC	-	Not Connect		-	78	NC	-	Not Connect	-	-
79	GND	-	Ground	N	-	80	NC	-	Not Connect	-	-
81	NC	-	Not Connect	-	-	82	NC	-	Not Connect	-	-
83	AUD_MCLK	JTAG_TMS	I2S Master CLK	Y	+3,3V	84	NC	-	Not Connect	-	-
85	nRESET	POR	Reset signal	N	-	86	NC	-	Not Connect	-	-
87	GND	-	Ground	N	-	88	CAN1_TX *4)*	UART3_CTS	CAN TX	Y	+3,3V
89	nSD_BOOT	-	-	N	-	90	CAN1_RX *4)*	UART3_RTS	CAN RX	Y	+3,3V

Table 2

B -CONNECTOR J2

ODD	NAME	PAD on i.MX	DESCRIPTION	GPIO	Voltage	EVEN	NAME	PAD on i.MX	DESCRIPTION	GPIO	Voltage
1	UART8_TXD *1)*	LCD_DATA20	UART TX OUT	Y	+3,3V	2	DISP0_D10 *1) 3)*	LCD_DATA10	LCD parallel signal	Y	+3,3V
3	UART8_RXD *1)*	LCD_DATA21	UART RX IN	Y	+3,3V	4	DISP0_D15 *1) 3)*	LCD_DATA15	LCD parallel signal	Y	+3,3V
5	GND	-	Ground	N	-	6	DISP0_D11 *1) 3)*	LCD_DATA11	LCD parallel signal	Y	+3,3V
7	GND	-	Ground	N	-	8	DISP0_D12 *1) 3)*	LCD_DATA12	LCD parallel signal	Y	+3,3V
9	ENET_MDC	GPIO1_IO07	ENET2 MDC signal	N *5)*	+3,3V	10	DISP0_D13 *1) 3)*	LCD_DATA13	LCD parallel signal	Y	+3,3V
11	ENET_MDIO	GPIO1_IO06	ENET2 MDIO signal	N *5)*	+3,3V	12	DISP0_D14 *1) 3)*	LCD_DATA14	LCD parallel signal	Y	+3,3V
13	nETH_LINK	-	Link led driver	N	+3,3V_ETH	14	DISP0_D9 *1) 3)*	LCD_DATA09	LCD parallel signal	Y	+3,3V
15	+3V3_ETH	-	Power in	N	-	16	DISP0_D2 *1) 3)*	LCD_DATA02	LCD parallel signal	Y	+3,3V
17	+3V3_ETH	-	Power in	N	-	18	DISP0_D3 *1) 3)*	LCD_DATA03	LCD parallel signal	Y	+3,3V
19	+3V3_ETH	-	Power in	N	-	20	DISP0_D8 *1) 3)*	LCD_DATA08	LCD parallel signal	Y	+3,3V
21	ETH0_RXP	-	Fast Ethernet RXP signal	N	+3,3V_ETH	22	DISP0_D4 *1) 3)*	LCD_DATA04	LCD parallel signal	Y	+3,3V
23	ETH0_RXN	-	Fast Ethernet RXN signal	N	+3,3V_ETH	24	DISP0_D1 *1) 3)*	LCD_DATA01	LCD parallel signal	Y	+3,3V
25	ETH0_TXP	-	Fast Ethernet TXP signal	N	+3,3V_ETH	26	DISP0_D0 *1) 3)*	LCD_DATA00	LCD parallel signal	Y	+3,3V
27	ETH0_TXN	-	Fast Ethernet TXN signal	N	+3,3V_ETH	28	DISP0_D6 *1) 3)*	LCD_DATA06	LCD parallel signal	Y	+3,3V
29	nETH_ACT	-	Activity led driver	N	+3,3V_ETH	30	DISP0_D5 *1) 3)*	LCD_DATA05	LCD parallel signal	Y	+3,3V
31	GND	-	Ground	N	-	32	DISP0_D16 *1) 3)*	LCD_DATA16	LCD parallel signal	Y	+3,3V
33	NC	-	Not Connect	-	-	34	DISP0_D17 *1) 3)*	LCD_DATA17	LCD parallel signal	Y	+3,3V
35	GPIO2_IO10	ENET2_RX_EN	General GPIO	Y	+3,3V	36	DISP0_D7 *1) 3)*	LCD_DATA07	LCD parallel signal	Y	+3,3V
37	GPIO2_IO09	ENET2_RX_DATA1	General GPIO	Y	+3,3V	38	DISP0_HSYNC *3)*	LCD_HSYNC	LCD parallel signal	Y	+3,3V
39	GPIO3_23 *1)*	LCD_DATA18	General GPIO	Y	+3,3V	40	DISP0_VSYNC *3)*	LCD_VSYNC	LCD parallel signal	Y	+3,3V
41	GPIO2_IO15	ENET2_RX_ER	General GPIO	Y	+3,3V	42	DISP0_DRDY *3)*	LCD_ENABLE	LCD parallel signal	Y	+3,3V
43	GPIO2_IO11	ENET2_TX_DATA0	General GPIO	Y	+3,3V	44	DISP0_CLK *3)*	LCD_CLK	LCD parallel signal	Y	+3,3V
45	GPIO2_IO13	ENET2_TX_EN	General GPIO	Y	+3,3V	46	GND	-	Ground	N	-
47	GPIO3_27 *1)*	LCD_DATA22	General GPIO	Y	+3,3V	48	GND	-	Ground	N	-
49	GPIO3_24 *1)*	LCD_DATA19	General GPIO	Y	+3,3V	50	NC	-	Not Connect		-

ODD	NAME	PAD on i.MX	DESCRIPTION	GPIO	Voltage	EVEN	NAME	PAD on i.MX	DESCRIPTION	GPIO	Voltage
51	GPIO3_28 1)	LCD_DATA23	General GPIO	Y	+3,3V	52	NC	-	Not Connect		-
53	GPIO2_IO14	ENET2_TX_CLK	General GPIO	Y	+3,3V	54	GND	-	Ground	N	-
55	GPIO2_IO08	ENET2_RX_DATA0	General GPIO	Y	+3,3V	56	NC	-	Not Connect		-
57	GPIO2_IO12	ENET2_TX_DATA1	General GPIO	Y	+3,3V	58	GND	-	Ground	N	-
59	GPIO4_14	NAND_CE1	General GPIO	Y	+3,3V	60	GND	-	Ground	N	-
61	GPIO3_4	LCD_RESET	General GPIO	Y	+3,3V	62	I2C1_SCL	CSI_PIXCLK	I2C signal (pull-up needed on carrier)	Y	+3,3V
63	GND	-	Ground	N	-	64	I2C1_SDA	CSI_MCLK	I2C signal (pull-up needed on carrier)	Y	+3,3V
65	GND	-	Ground	N	-	66	GND	-	Ground	N	-
67	PWM5_OUT	NAND_DQS	Spare PWM	Y	+3,3V	68	eCSPI1_SCLK	CSI_DATA04	SPI clock	Y	+3,3V
69	GND	-	Ground	N	-	70	eCSPI1_SS0	CSI_DATA05	SPI Slave select	Y	+3,3V
71	GND	-	Ground	N	-	72	eCSPI1_MOSI	CSI_DATA06	SPI MOSI	Y	+3,3V
73	SDIO_DET	UART1_RTS	USDHC1 CD	Y	+3,3V	74	eCSPI1_MISO	CSI_DATA07	SPI MISO	Y	+3,3V
75	SD2_DET	UART1_CTS	USDHC2 CD	Y	+3,3V	76	GND	-	Ground	N	-
77	SD2_D1	CSI_DATA01	uSDHC2 DAT 1 signal	Y	+3,3V	78	SD1_D3	SD1_DATA3	uSDHC1 DAT 3 signal	Y	+3,3V
79	SD2_D0	CSI_DATA00	uSDHC2 DAT 0 signal	Y	+3,3V	80	SD1_D1	SD1_DATA1	uSDHC1 DAT 1 signal	Y	+3,3V
81	SD2_D3	CSI_DATA03	uSDHC2 DAT 3 signal	Y	+3,3V	82	SD1_D2	SD1_DATA2	uSDHC1 DAT 2 signal	Y	+3,3V
83	SD2_D2	CSI_DATA02	uSDHC2 DAT 2 signal	Y	+3,3V	84	SD1_D0	SD1_DATA0	uSDHC1 DAT 0 signal	Y	+3,3V
85	SD2_CLK	CSI_VSYNC	USDHC2 Clock signal	Y	+3,3V	86	SD1_CLK	SD1_CLK	uSDHC1 Clock signal	Y	+3,3V
87	SD2_CMD	CSI_HSYNC	uSDHC2 cmd signal	Y	+3,3V	88	SD1_CMD	SD1_CMD	uSDHC1 cmd signal	Y	+3,3V
89	GND	-	Ground	N	-	90	GND	-	Ground	N	-

Table 3

The yellow rows highlight the required minimum electrical connections in order to make the module working correctly.

*1) Note: for the use of this pin refer to boot option in "**5.12.1 Boot Signals Management**" chapter*

2) Connect to Coin-Cell or Super-Cap; left floating if not used

3) LCD peripheral not available on modules equipped with MCIMX6Y1, LCD pins can be used as GPIO and other functions

4) CAN bus not available on modules equipped with MCIMX6Y7

5) WARNING!
Pin used on the SOM's internal PHY! The use as GPIO impair the functionality of the main Ethernet peripheral.
***We recommend to use this pin only for ENET function**. For further details please see chapter* 5.6.1 Second Ethernet i/f

4.2 ELECTRICAL SPECIFICATIONS

	V Min (Volts)	V Typ (Volts)	V Max (Volts)
Vin [1)]	+ 2,8	+ 3,3	+ 3,5
VBUS_OTG_USB, VBUS_USB	+ 4,70	+5	+ 5,35
GPIO V(oh)	+ 3,15	-	-
GPIO V(ol)	-	-	+ 0,15
GPIO V(ih)	+ 2,35		+ 3,3
GPIO V(il)	0	-	+ 1

Table 4

1) This measure has done testing the module's start at the limit temperatures of -40°C and +85°C

Module	Test condition	Current Min @Vin	Current Typ @Vin	Current Max @Vin
MicroGEA	Linux Sleep mode (+3V3_ETH= 0V)	-	4 mA	4.5 mA
	Linux (only standard services running)	-	130 mA	155 mA
	QT, 2D dynamic graphic application running	240 mA	250 mA	290 mA

Table 5

CHAPTER 5

5. CARRIER BOARD DESIGN

This Chapter gives the technical specifications for carrier board design.

Section includes：

- ✓ **Carrier Board recommendations**
- ✓ **Power signals and backup battery**
- ✓ **Serials**
- ✓ **CAN Bus**
- ✓ **Ethernet**
- ✓ **USB**
- ✓ **SDIO**
- ✓ **LCD**
- ✓ **EPD**
- ✓ **Resistive Touch screen**
- ✓ **Boot mode**
- ✓ **Audio**
- ✓ **Reset pin management**

5.1 CARRIER BOARD RECOMMENDED SPECIFICATIONS

5.1.1 PLANARITY IN FINISH PROCESS

Due to the technical and mechanical specifications of the connector we suggest the maximum planarity of the footprint on PCB, so we suggest a type of finish obtained by horizontal process (we suggest and use for our carrier boards a type Chemical Gold finish).

5.1.2 PLANARITY OF PCB

Also the planarity of the entire Printed Circuit Board must be kept in check especially when the carrier board grows in size. In this case we suggest you contact the manufacturer of PCB to understand how improve the planarity of ended board and optimize the process maintaining the electrical characteristics unchanged

5.1.3 POWER SUPPLY

It's strongly recommended that the power supply of the carrier board, which feeds the driver and control devices connected with the i.MX processor, begins to work after the initialization of the processor itself

5.1.4 MODULE POSITIONING AND FIXING

Following, the mechanical positioning of the connectors on the carrier board used to insert the MicroGEA module

During the insertion pay attention to respect the direction given by the outline of the module and the silkscreen on the carrier board (see the red circle in the figure)

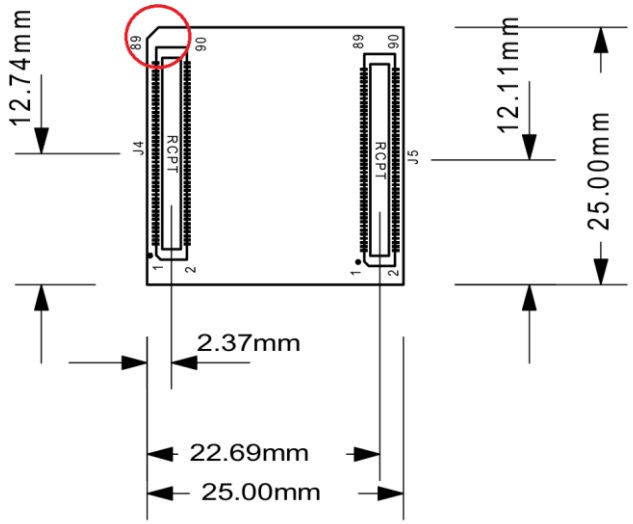


Figure 3

Note: For information about carrier's connector code and specifications, refer to Chapter 2.4.

5.2 HOW TO POWER THE MODULE

Read carefully the related sections before starting the power stage design. This module needs to be supplied with a +3.3Vin power. Refer to the table below for the power supply range specification. The power dissipated by the module in the operating mode is about 200 mA, but **the system must provide at least a power of 1A at 3.3V to allow the start of the module.**

In the following table are shown the module power supply pins numbering. Connect all power supply pins in order to avoid damage.

A connector	B connector	Name	Primary Function Description	GPIO Capable	Voltage
19	-	+3,3V	Power PIN	N	-
20	-	+3,3V	Power PIN	N	-
21	-	+3,3V	Power PIN	N	-
22	-	+3,3V	Power PIN	N	-
1	5	GND	Power PIN	N	-
11	7	GND	Power PIN	N	-
16	31	GND	Power PIN	N	-
32	46	GND	Power PIN	N	-
44	48	GND	Power PIN	N	-
45	54	GND	Power PIN	N	-
61	58	GND	Power PIN	N	-
63	60	GND	Power PIN	N	-
68	63	GND	Power PIN	N	-
72	65	GND	Power PIN	N	-
79	66	GND	Power PIN	N	-
87	69	GND	Power PIN	N	-
-	71	GND	Power PIN	N	-
-	76	GND	Power PIN	N	-
-	89	GND	Power PIN	N	-
-	90	GND	Power PIN	N	-

Table 6

5.2.1 HOW TO CONNECT A BACKUP BATTERY

The module allows the use of lithium rechargeable battery or supercapacitor as backup battery.
The connection with module is obtained by connecting directly the backup battery to the +Vcoin signal (pin 18 floating if not used).

WARNING: the RTC current consumption measured during the supply by the Vcoin can reach 450uA.

Note: *The module is already designed to manage the charge of backup battery.*

For further details on the power supply refer to "i.MX 6ULL" Data Sheet and Reference Manual.

5.3 HOW TO CONNECT TWO 2-WIRE RS232 SERIAL PORT

This section shows how to use the UART1 and UART5 as 2-wire RS232 serial ports.
The following table shows the UART1 and UART5 pins numbering.

A Connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
75	UART5_TXD	UART TXD signal	UART5_TX_DATA	Y	+3,3V
73	UART5_RXD	UART RXD signal	UART5_RX_DATA	Y	+3,3V
28	UART1_TXD	OS Console TX	UART1_TX_DATA	Y	+3,3V
26	UART1_RXD	OS Console RX	UART1_RX_DATA	Y	+3,3V

Table 7

The signal on the module's UART pins is 3.3V logic level, this cannot be connected directly to a RS232 device like a PC Serial port, the use of a transceiver on the base board is mandatory in order to avoid module damage.

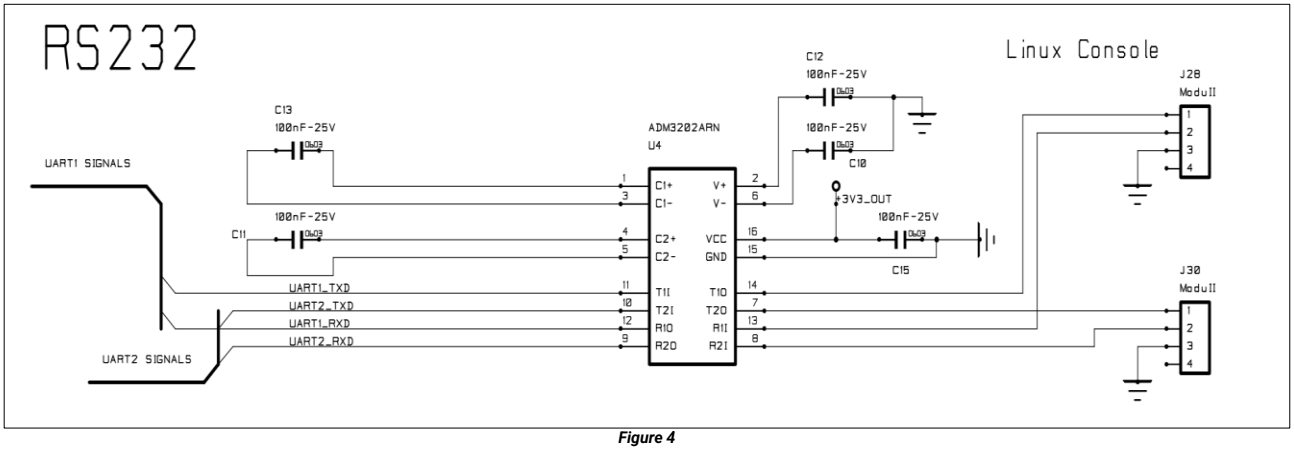


Figure 4

In this example an ADM3202ARN IC from Analog Device is used like transceiver for both UART without any control signal. In case RTS and CTS are need, a transceiver must be used for these signals.

When Linux is installed on a module, UART1 is used like console. The default communications settings are shown in the table below.

Linux console default settings	
Baud rate	115200
Data length	8 bit
Parity	none
Stop	1bit

Table 8

* **Note**: *the CONUART is used as Linux Console*

5.4 HOW TO CONNECT A RS485 SERIAL PORT

This chapter is shows how an RS485 serial port can be connected to the module. The figure below shows how UART3 is used to connect to a RS485 transceiver on the starter kit. The figure shows UART3 connection but you can consider that also UART 4 & 5 can be used to connect a RS485 transceiver.

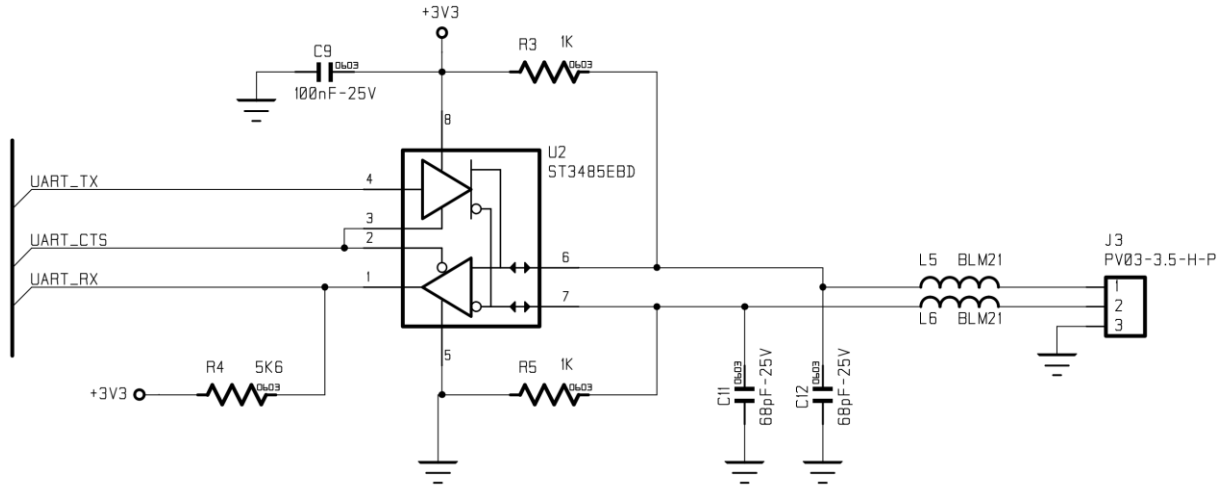


Figure 5

The pins involved in this RS485 communication example are listed in the following table.

A Connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
71	UART2 CTS	UART2 CTS signal Output	UART2 CTS	Y	+3,3V
69	UART2 RTS	UART2 RTS signal Input	UART2 RTS	Y	+3,3V
67	UART2 TXD	UART2 TXD signal Output	UART2 TX_DATA	Y	+3,3V
65	UART2 RXD	UART2 RXD signal Input	UART2 RX_DATA	Y	+3,3V

Table 9

5.5 HOW TO CONNECT CAN BUS INTERFACES

This chapter describes how CAN bus transceiver can be connected to a module. The figure below shows how CAN bus1 and 2 are connected in the evaluation board. Both CAN buses have been implemented.

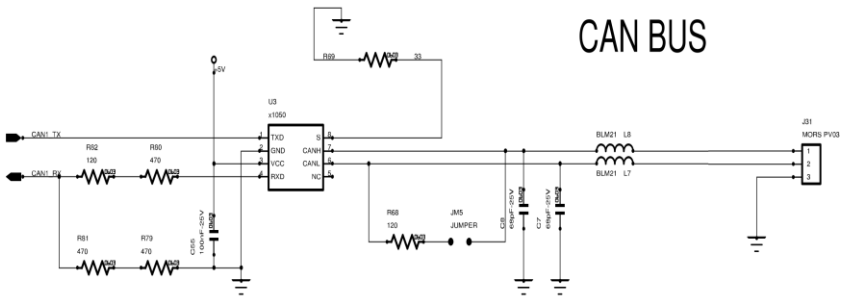


Figure 6

The following table describes the pins' numbering in the main connector involved in the CAN interface

A Connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
88	CAN1_TX	CAN 1 transmit signal	UART3_CTS	Y	+3,3V
90	CAN1_RX	CAN 1 receive signal	UART3_RTS	Y	+3,3V

Table 10

The Jumpers JM1, is used to close the load of the CAN Bus to 120 Ω

Note: CAN peripheral not available on module* equipped with *CPU MCIMX6Y7

5.6 HOW TO DESIGN THE ETHERNET INTERFACE

The NXP i.MX6UL Ethernet Media Access Controller (MAC) is designed to support both 10 and 100 Mbps Ethernet/IEEE standard 802.3™ networks. The 10-Mbps and 100-Mbps RMII Ethernet physical interfaces is supported. The figure shows how to connect the Ethernet interface to module.

50 Ohm PU termination resistors for the Ethernet TX/RX pairs are already present on the SOM. It is not necessary to place them on the carrier board

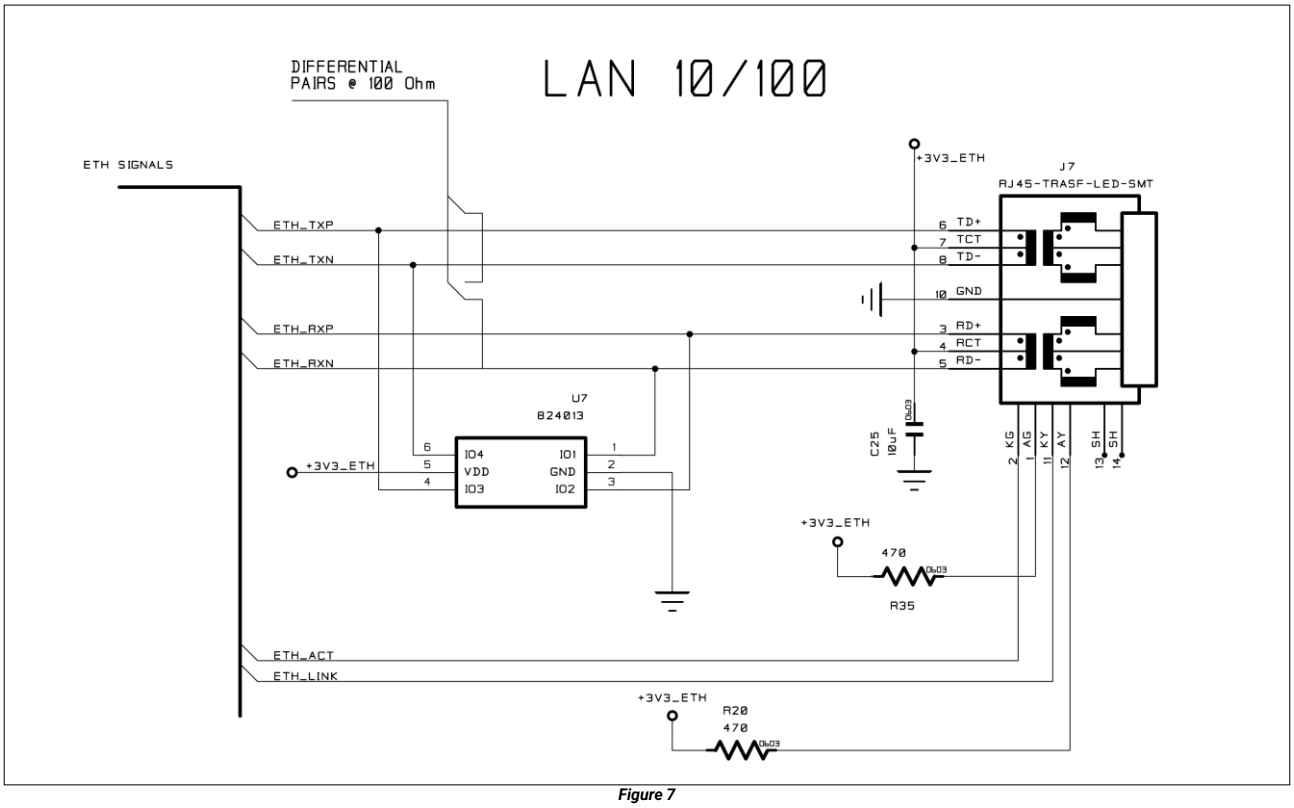


Figure 7

The table below lists all Ethernet signal of the module:

B Connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
27	ETH_TXN	Fast Ethernet TXN signal	-	-	+3,3V_ETH
25	ETH_TXP	Fast Ethernet TXP signal	-	-	+3,3V_ETH
23	ETH_RXN	Fast Ethernet RXN signal	-	-	+3,3V_ETH
21	ETH_RXP	Fast Ethernet RXP signal	-	-	+3,3V_ETH
13	ETH_LINK#	Link led driver	-	-	+3,3V_ETH
29	ETH_ACT#	Activity led driver	-	-	+3,3V_ETH

Table 11

*** *Note:*** If not used, this pin must be left floating.

In order to reduce the module consume during the power down Engicam provides the module with the pin 3V3_ETH that give the user the possibility to switch off the Ethernet PHY during this working mode (command echo mem > /sys/class/power/state).
These pins 15, 17, 19 of the B Connector (J2) can be connected, on the carrier board, to the 3V3 using a circuitry as follows.

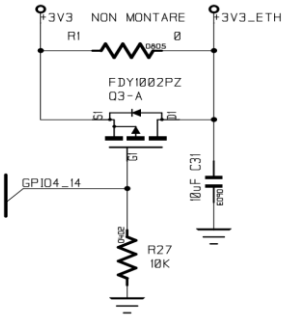


Figure 8

The system is under validation otherwise it's strongly recommended to plan a bypass circuitry (e.g. R1 in the figure) to allow the direct connection of 3V3_ETH with +3V3

To optimize the SOM current consumption during power down state Engicam has arranged the power supply of the PHY Ethernet to work independently by the rest of the module
For this reason a 3V3_ETH pin is available on B connector. The pins can be connected as shown in the figure to allow to the signal GPIO4_14 to switch off the Phy Ethernet using the command

echo mem > /sys/class/power/state

that puts the module into a power down state

This system has yet to be validated, so it is advisable to mount the circuit of a bypass system to the enclosure, see 0 ohm resistor "not mount" in the figure

5.6.1 SECOND ETHERNET I/F

The module MicroGEA allows to enable a second Ethernet by adding a PHY device on the carrier board and connecting to the processor by the ENET2 interface.

The J2 connector provides the second Ethernet peripheral mapped as follows

B Connector	Name	CPU Pin Name	Voltage
43	GPIO2_IO11	ENET2_TX_DATA0	+3,3V
57	GPIO2_IO12	ENET2_TX_DATA1	+3,3V
45	GPIO2_IO13	ENET2_TX_EN	+3,3V
53	GPIO2_IO14	ENET2_TX_CLK	+3,3V
55	GPIO2_IO08	ENET2_RX_DATA0	+3,3V
37	GPIO02_IO09	ENET2_RX_DATA1	+3,3V
41	GPIO2_IO15	ENET2_RX_ER	+3,3V
35	GPIO02_IO10	ENET2_RX_EN	+3,3V
9	ENET_MDC [1)]	GPIO01_IO06	+3,3V
11	ENET_MDIO [1)]	GPIO01_IO07	+3,3V

Table 12

[1)] This signal is used to drive the PHY of the main Ethernet interface available on the module. It is possible to use this signal to drive also a second optional PHY (to be added on the carrier board) and to enable a second Ethernet interface.

If not used for the second Ethernet interface is strongly recommended to leave these pins NC.

For any questions, please contact us at support@engicam.com

5.6.2 COMPONENT PLACEMENT CONSIDERATIONS

Components placement can affect signal quality, emissions and can decrease EMI problems.

1. If the magnetics are a discrete component than the distance from the connector RJ45 should be kept to under 25mm of separation.
2. To decrease EMI problems the distance between magnetics and Phy should be at least 25mm or greater to isolate the PHY from magnetics.
3. The distance between Phy and RJ45 connector should always be within 200 mm.
4. The differential transmit pair should be keep at least 25mm from the edge of PCB up to the magnetics. If the magnetics are integrated into RJ45 the differential pair should be routed to the back of integrated magnetics RJ45 connector , away from the board of PCB.
5. The 49.9 ohm pull-up resistors on the differential lines should be placed within 10 mm of the Phy device
6. The signals RX & TX should be independently matched in length to within 6mm

See the following figure

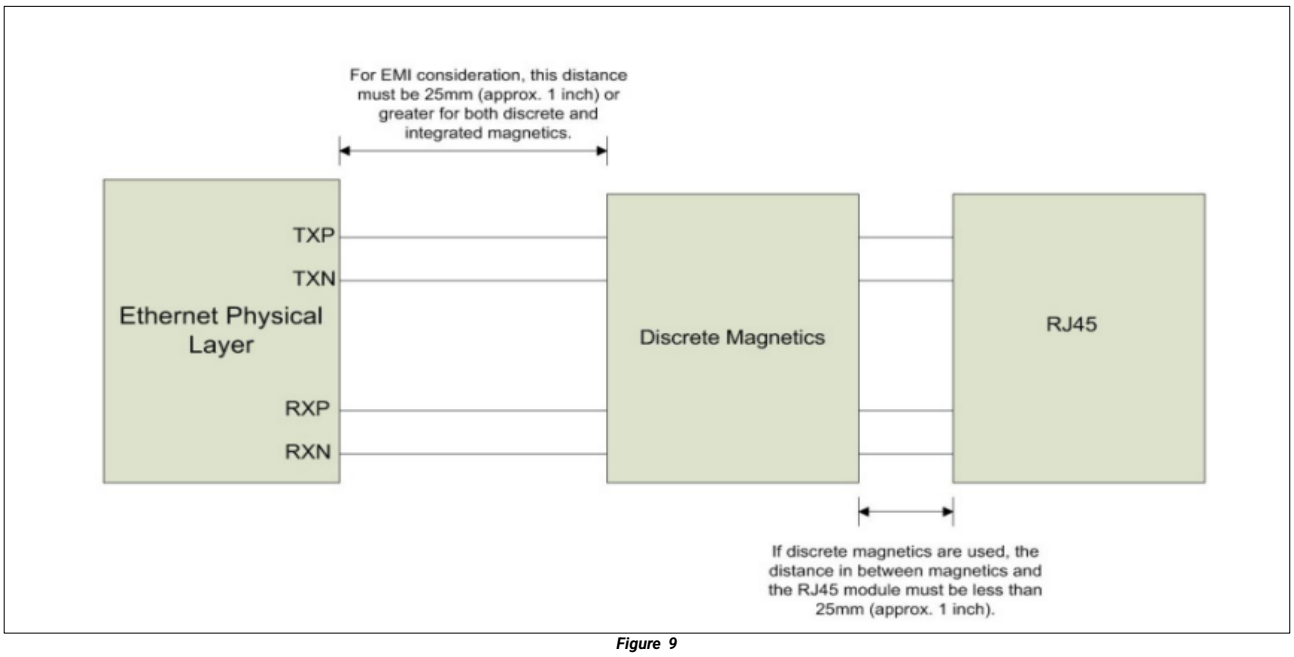


Figure 9

The PHY used in the module is the ***SMSC LAN8710***.
For more information refer to the ***SMSC Ethernet Physical Layer Layout Guidelines***.

For a list of magnetics selected to operate with the SMSC LAN8710, refer to the Application note ***AN 8-13 Suggested Magnetics.***

*** this is figure 2.3 from SMSC Ethernet Physical Layer Layout Guidelines**

5.6.3 CABLE TRANSIENT EVENT AND PHY PROTECTION

Cable transient events are + and - DC surges that are induced across the transformer onto the PHY side of the TX+/- and RX+/- signals as shown in the figure below. The PHY side of the transformer should not contain any DC component other than the typical 3.3V pull-up on the center tap of the transformer for analog signal biasing. Especially in POE applications, there are two main reasons why cable transient events occur, negative rail PSE switching, and hot unplug/plug-in events.

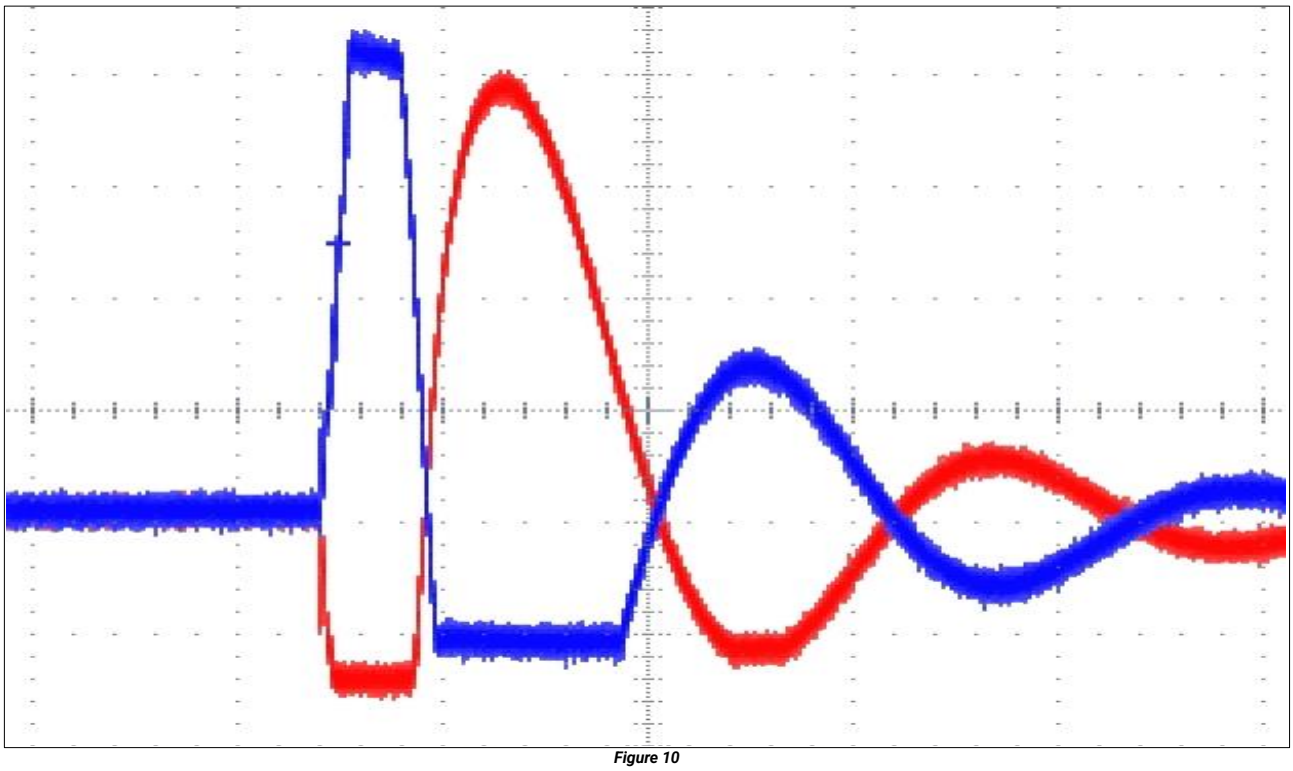


Figure 10

Transient observer on the PHY side of Eth Magnetics

Scale X = 1uS/div

Scale Y = 5V/div

Note: *for further details about Cable transient events refer to file AN1718 of SMSC*

5.6.4 PHY ETHERNET

When using an SMSC device, for each application an external transient protection is recommended, especially when the POE is used, as shown in figure below. The schematic shows an example of a TVS suppression solution. This solution couples the energy differentially into the two TVS diodes on each differential pair. For cases when the transient is across the TX+/- pair in the figure below, the voltage is clamped at a value equivalent to the forward bias voltage across D1, plus the zener voltage of D2. This transient voltage must be clamped at a voltage no **greater than 5V**. D3 and D4 act the same way when the transient is across the RX+/- differential pair. The total capacitance seen by each differential pair must not exceed 50pF (25pF single ended).

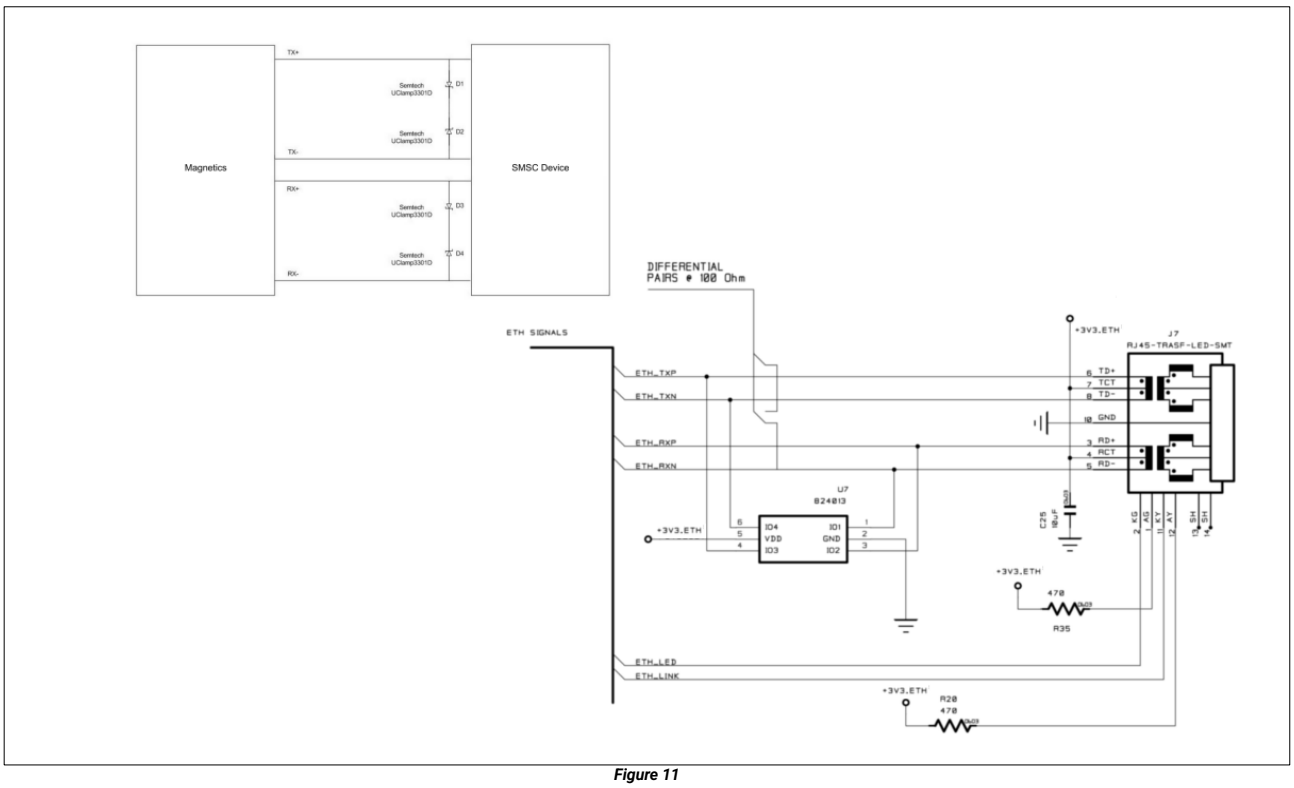


Figure 11

Recommended by ENGICAM:

Diode array recommended by ENGICAM for protection is **Wurth Elektronik 824015043** (TVS, 4 CH, ESD, 3.3V).

Note: *for further details about PHY Protection refer to file AN1718 of SMSC*

5.7 USB INTERFACE

5.7.1 HOW TO CONNECT THE USB OTG INTERFACE

The NXP i.MX6UL USB module provides high performance USB On-The-Go (up to 480Mbps), compatible with the USB 2.0 specification. An OTG HS PHY is also integrated so no external OTG PHY is needed on the baseboard. The figure shows how the MINI-AB USB/OTG connector is powered and connected in the evaluation board. In the following table are listed all USB/OTG signal of mail connector.

Use of the USB OTG port as Device or as Host depending on the status of the ID signal that is used also to enable the power supply.

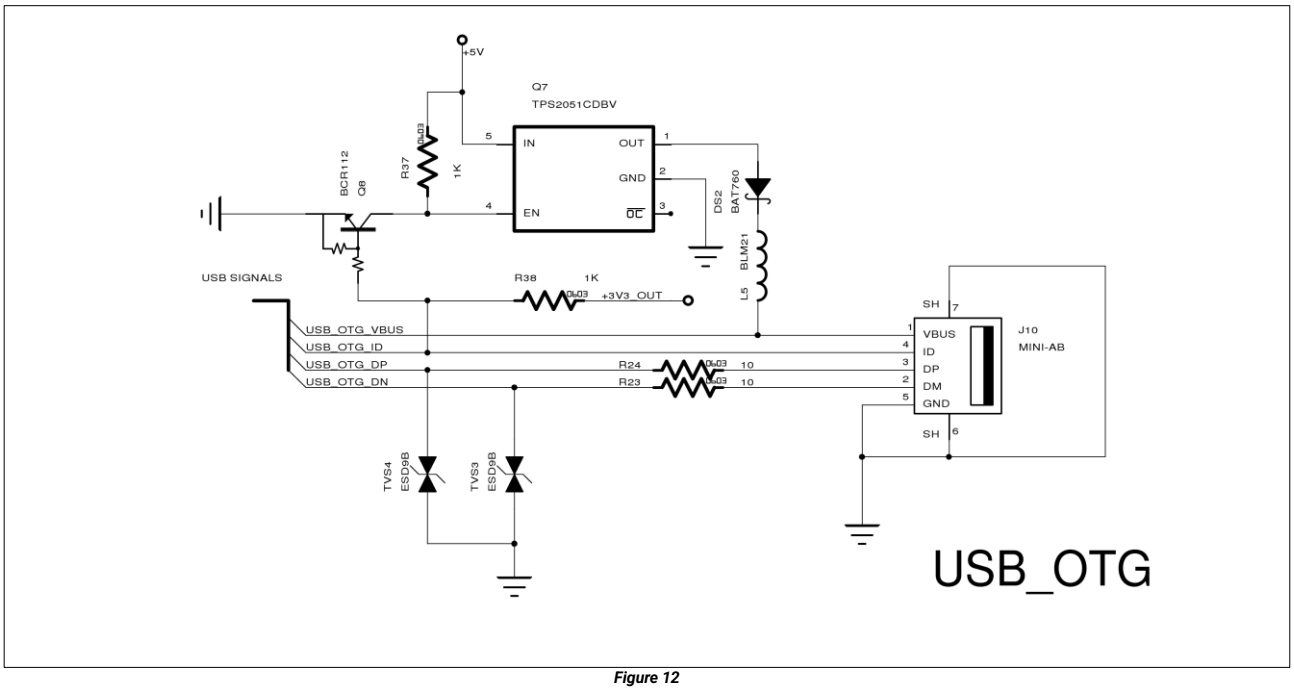


Figure 12

A Connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
12	USB_OTG_VBUS *	USB on the go interface	USB_OTG1_VBUS	N	-
6	USB_OTG_DP	USB on the go interface	USB_OTG1_DP	N	-
4	USB_OTG_DN	USB on the go interface	USB_OTG1_DN	N	-
2	USB_OTG_ID	USB on the go interface	UART3_TX_DATA	N	-

Table 12

**** Note: The USB_OTG_VBUS is an INPUT power signal. It must be connected to +5V***

The following figures show two different ways to connect the USB OTG interface that may be used to work as either a host or a device.

Use of the USB OTG port as a **Host** with its own dedicated supply. The ID signal is forced to GND.

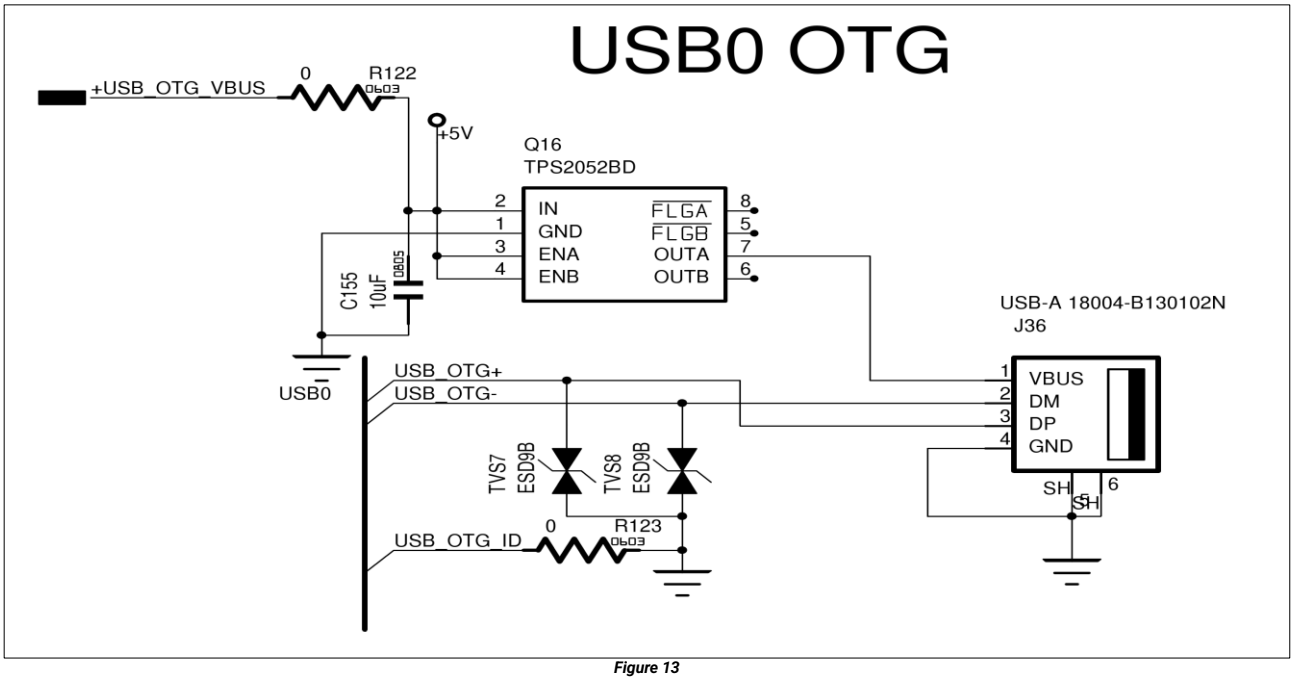


Figure 13

Use of the USB OTG port as **Device.**

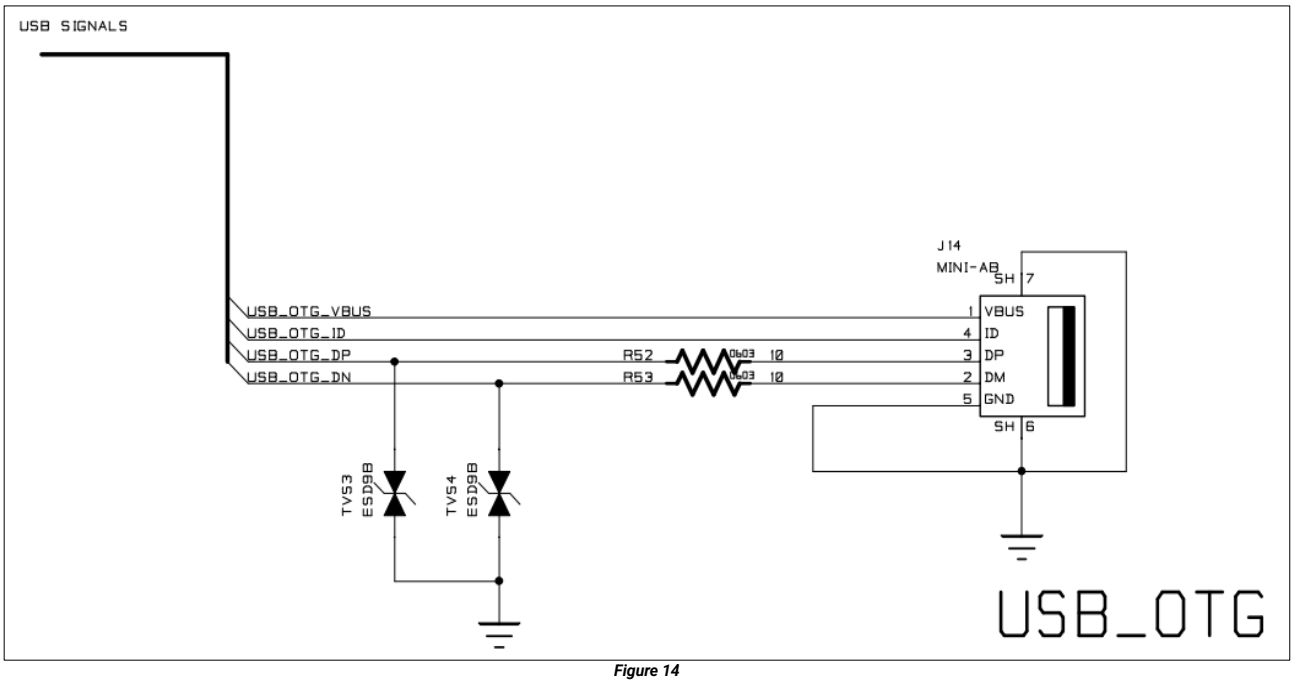


Figure 14

5.7.2 HOW TO CONNECT THE USB HOST INTERFACE

The module provides one port for USB host interface. The figure shows how to connect this port to the Module.

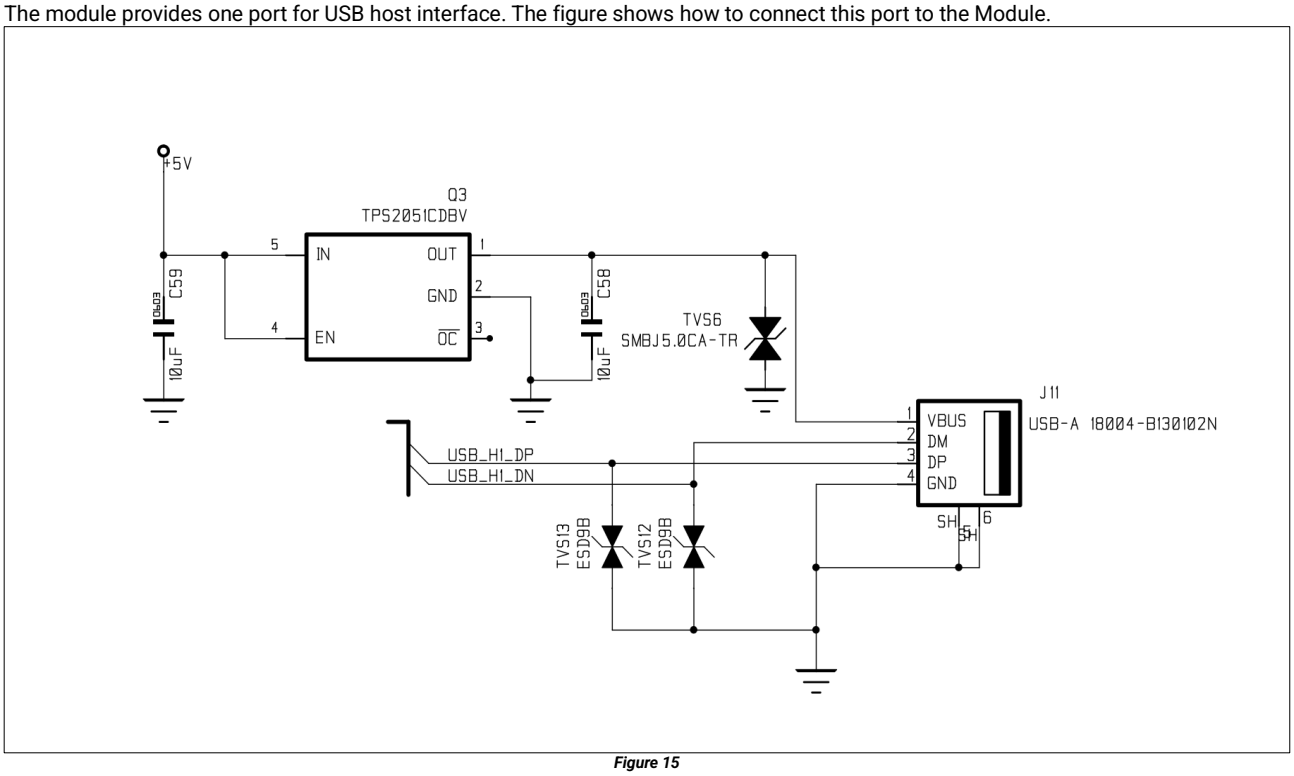


Figure 15

A Connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
14	USB_VBUS *	USB HOST interface	USB_OTG2_VBUS	N	-
10	USB_DP	USB HOST interface	USB_OTG2_DP	N	-
8	USB_DN	USB HOST interface	USB_OTG2_DN	N	-

Table 13

**** Note: The USB_VBUS is an INPUT power signal. It must be connected to a 5V source if USB is used.***

5.8 HOW TO CONNECT THE SD CARD INTERFACE

The NXP i.MX6UL Ultra Secured Digital Host Controller (uSDHC) provides the interface between the host system and MMC/SD/SDIO cards, including cards with reduced size or mini cards. The module includes these features and the figure shows how the Micro SD Card connector is connected to MicroGEA Module in the evaluation board. The uSDHC signal of the module's main connector are listed in the table below.

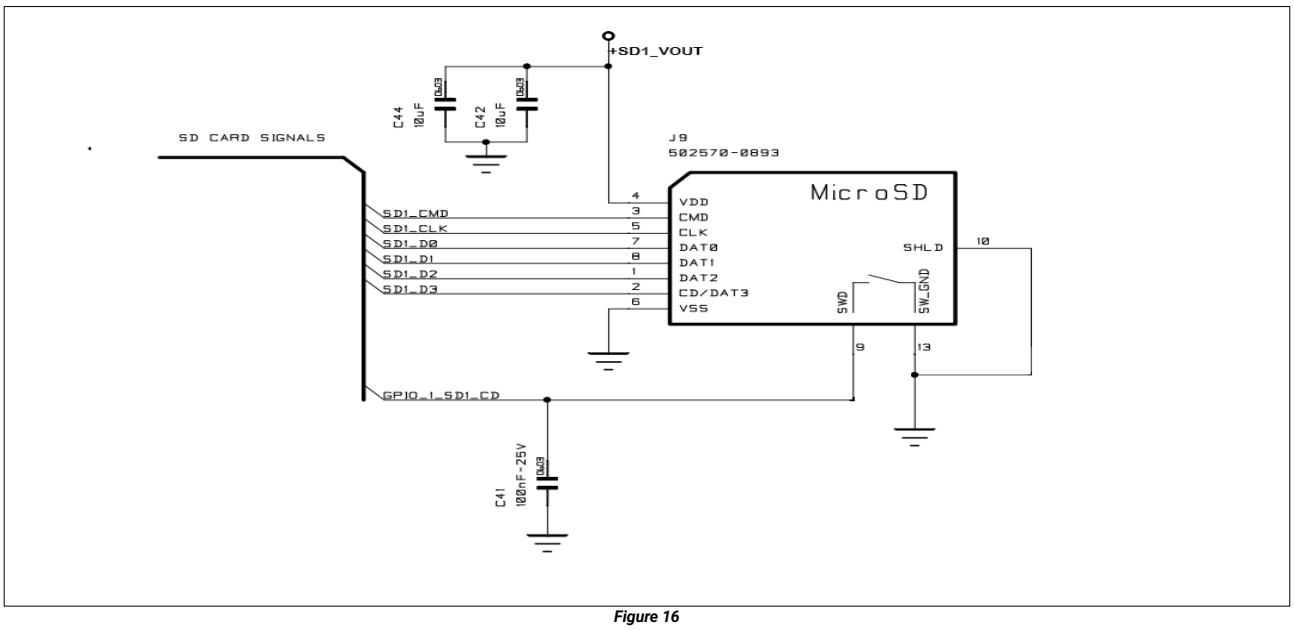


Figure 16

B Connector	Name	Primary Function Description	CPU Pin Name	GPIO Capable	Voltage
73	SDIO_DET	uSDHC CD Signal	UART1_RTS	Y	+3,3V
84	SD1_DAT0	uSDHC DAT 0 signal	SD1_DATA0	Y	+3,3V
80	SD1_DAT1	uSDHC DAT 1 signal	SD1_DATA1	Y	+3,3V
82	SD1_DAT2	uSDHC DAT 2 signal	SD1_DATA2	Y	+3,3V
78	SD1_DAT3	uSDHC DAT 3 signal	SD1_DATA3	Y	+3,3V
86	SD1_CLK	uSDHC CLK signal	SD1_CLK	Y	+3,3V
88	SD1_CMD	uSDHC CMD signal	SD1_CMD	Y	+3,3V

Table 14

5.9 HOW TO CONNECT AN LCD DISPLAY

5.9.1 CONNECTION MAP FOR 18 BIT DISPLAY

The following map represent the connection mode applied to 18 bit TFT display.
For every connection the colour controlled is joined

A Connector	B Connector	Name	Primary Function Description	CPU Pin Name	18 bit TFT	GPIO Capable	Voltage
	26	DISP0_D0	LCD interface	LCD_DATA00	BLU 0	Y	+3,3V
	24	DISP0_D1	LCD interface	LCD_DATA01	BLU 1	Y	+3,3V
	16	DISP0_D2	LCD interface	LCD_DATA02	BLU 2	Y	+3,3V
	18	DISP0_D3	LCD interface	LCD_DATA03	BLU 3	Y	+3,3V
	22	DISP0_D4	LCD interface	LCD_DATA04	BLU 4	Y	+3,3V
	30	DISP0_D5	LCD interface	LCD_DATA05	BLU 5	Y	+3,3V
	28	DISP0_D6	LCD interface	LCD_DATA06	GREEN 0	Y	+3,3V
	36	DISP0_D7	LCD interface	LCD_DATA07	GREEN 1	Y	+3,3V
	20	DISP0_D8	LCD interface	LCD_DATA08	GREEN 2	Y	+3,3V
	14	DISP0_D9	LCD interface	LCD_DATA09	GREEN 3	Y	+3,3V
	2	DISP0_D10	LCD interface	LCD_DATA10	GREEN 4	Y	+3,3V
	6	DISP0_D11	LCD interface	LCD_DATA11	GREEN 5	Y	+3,3V
	8	DISP0_D12	LCD interface	LCD_DATA12	RED 0	Y	+3,3V
	10	DISP0_D13	LCD interface	LCD_DATA13	RED 1	Y	+3,3V
	12	DISP0_D14	LCD interface	LCD_DATA14	RED 2	Y	+3,3V
	4	DISP0_D15	LCD interface	LCD_DATA15	RED 3	Y	+3,3V
	32	DISP0_D16	LCD interface	LCD_DATA16	RED 4	Y	+3,3V
	34	DISP0_D17	LCD interface	LCD_DATA17	RED 5	Y	+3,3V
	38	DISP0_HSYNC	LCD interface	LCD_HSYNC		Y	+3,3V
	40	DISP0_VSYNC	LCD interface	LCD_VSYNC		Y	+3,3V
	42	DISP0_DRDY	LCD interface	LCD_ENABLE		Y	+3,3V
	44	DISP0_CLK	LCD interface	LCD_CLK		Y	+3,3V
52		LCD_BKL_PWM	LCD BKL control	ENET1_RX_ER		Y	+3,3V

Table 15

5.9.2 CONNECTION MAP FOR 24 BIT DISPLAY

The following map represent the connection mode applied to 24 bit TFT display.
For every connection the colour controlled is joined

A Connector	B Connector	Name	Primary Function Description	CPU Pin Name	24 bit TFT	GPIO Capable	Voltage
	26	DISP0_D0	LCD interface	LCD_DATA00	BLU 0	Y	+3,3V
	24	DISP0_D1	LCD interface	LCD_DATA01	BLU 1	Y	+3,3V
	16	DISP0_D2	LCD interface	LCD_DATA02	BLU 2	Y	+3,3V
	18	DISP0_D3	LCD interface	LCD_DATA03	BLU 3	Y	+3,3V
	22	DISP0_D4	LCD interface	LCD_DATA04	BLU 4	Y	+3,3V
	30	DISP0_D5	LCD interface	LCD_DATA05	BLU 5	Y	+3,3V
	28	DISP0_D6	LCD interface	LCD_DATA06	BLU 6	Y	+3,3V
	36	DISP0_D7	LCD interface	LCD_DATA07	BLU 7	Y	+3,3V
	20	DISP0_D8	LCD interface	LCD_DATA08	GREEN 0	Y	+3,3V
	14	DISP0_D9	LCD interface	LCD_DATA09	GREEN 1	Y	+3,3V
	2	DISP0_D10	LCD interface	LCD_DATA10	GREEN 2	Y	+3,3V
	6	DISP0_D11	LCD interface	LCD_DATA11	GREEN 3	Y	+3,3V
	8	DISP0_D12	LCD interface	LCD_DATA12	GREEN 4	Y	+3,3V
	10	DISP0_D13	LCD interface	LCD_DATA13	GREEN 5	Y	+3,3V
	12	DISP0_D14	LCD interface	LCD_DATA14	GREEN 6	Y	+3,3V
	4	DISP0_D15	LCD interface	LCD_DATA15	GREEN 7	Y	+3,3V
	32	DISP0_D16	LCD interface	LCD_DATA16	RED 0	Y	+3,3V
	34	DISP0_D17	LCD interface	LCD_DATA17	RED 1	Y	+3,3V
	39	DISP0_D18	LCD interface	LCD_DATA18	RED 2	Y	+3,3V
	49	DISP0_D19	LCD interface	LCD_DATA19	RED 3	Y	+3,3V
	1	DISP0_D20	LCD interface	LCD_DATA20	RED 4	Y	+3,3V
	3	DISP0_D21	LCD interface	LCD_DATA21	RED 5	Y	+3,3V
	47	DISP0_D22	LCD interface	LCD_DATA22	RED 6	Y	+3,3V
	51	DISP0_D23	LCD interface	LCD_DATA23	RED 7	Y	+3,3V
	38	DISP0_HSYNC	LCD interface	LCD_HSYNC	-	Y	+3,3V
	40	DISP0_VSYNC	LCD interface	LCD_VSYNC	-	Y	+3,3V
	42	DISP0_DRDY	LCD interface	LCD_ENABLE	-	Y	+3,3V
	44	DISP0_CLK	LCD interface	LCD_CLK	-	Y	+3,3V
52		LCD_BKL_PWM	LCD BKL control	ENET1_RX_ER			Y

Table 16

Note: the LCD peripheral is not available on processor MCIMX6Y1 series

5.10 EPD INTERFACE

The following map represent the EPD connection. **EPD peripheral is available only for parts equipped with Y7 processors**

A Connector	B Connector	Name	Primary Function Description	CPU Pin Name	Voltage
9	-	EPDC_PWRCTRL01	Panel power control (sw controlled)	UART4_RX_DATA	+3,3V
52	-	EPDC_SDOEZ	Source driver output enable to zero	ENET1_RX_ER	+3,3V
73	-	EPDC_PWRCTRL03	Panel power control (sw controlled)	UART5_RX_DATA	+3,3V
75	-	EPDC_PWRCTRL02	Panel power control (sw controlled)	UART5_TX_DATA	+3,3V
-	1	EPDC_VCOM01	Panel VCOM	LCD_DATA20	+3,3V
-	2	EPDC_PWRCOM	Panel power control (sw controlled)	LCD_DATA10	+3,3V
-	4	EPDC_GDRL	Gate drive-shift direction	LCD_DATA15	+3,3V
-	6	EPDC_PWRSTAT	Panel power good state	LCD_DATA11	+3,3V
-	8	EPDC_PWRCTRL00	Panel power control (sw controlled)	LCD_DATA12	+3,3V
-	12	EPDC_SDSHR	Source driver shift dir	LCD_DATA14	+3,3V
-	14	EPDC_PWRWAKE	Panel power control wakw signal (sw controlled)	LCD_DATA09	+3,3V
-	20	EPDC_PWRIRQ	Panel power IRQ	LCD_DATA08	+3,3V
-	32	EPDC_GDCLK	gate drive clk	LCD_DATA16	+3,3V
-	34	EPDC_GDSP	gate drive start pulse	LCD_DATA17	+3,3V
-	38	EPDC_SDOE	Gate driver output enable	LCD_HSYNC	+3,3V
-	42	EPDC_SDLE	Source driver latch enable	LCD_ENABLE	+3,3V
-	44	EPDC_SDCLK	Source driver shift clk	LCD_CLK	+3,3V
-	49	EPDC_VCOM00	Panel VCOM	LCD_DATA19	+3,3V
-	61	EPDC_GDOE	gate driver output enable	LCD_RESET	+3,3V
-	10	EPDC_BDR00	Panel border control (sw controlled)	LCD_DATA13	+3,3V
-	39	EPDC_BDR01	Panel border control (sw controlled)	LCD_DATA18	+3,3V
-	40	EPDC_SDCE00	Source driver chip enable/start-pulse	LCD_VSYNC	+3,3V
-	3	EPDC_SDCE01	Source driver chip enable/start-pulse	LCD_DATA21	+3,3V
-	47	EPDC_SDCE02	Source driver chip enable/start-pulse	LCD_DATA22	+3,3V
-	51	EPDC_SDCE03	Source driver chip enable/start-pulse	LCD_DATA23	+3,3V
-	26	EPDC_SDDO00	source Driver Data	LCD_DATA00	+3,3V
-	24	EPDC_SDDO01	source Driver Data	LCD_DATA01	+3,3V
-	16	EPDC_SDDO02	source Driver Data	LCD_DATA02	+3,3V
-	18	EPDC_SDDO03	source Driver Data	LCD_DATA03	+3,3V
-	22	EPDC_SDDO04	source Driver Data	LCD_DATA04	+3,3V
-	30	EPDC_SDDO05	source Driver Data	LCD_DATA05	+3,3V
-	28	EPDC_SDDO06	source Driver Data	LCD_DATA06	+3,3V
-	36	EPDC_SDDO07	source Driver Data	LCD_DATA07	+3,3V
-	55	EPDC_SDDO08	source Driver Data	ENET2_RX_DATA0	+3,3V
-	37	EPDC_SDDO09	source Driver Data	ENET2_RX_DATA1	+3,3V
-	35	EPDC_SDDO10	source Driver Data	ENET2_RX_EN	+3,3V
-	43	EPDC_SDDO11	source Driver Data	ENET2_TX_DATA0	+3,3V
-	57	EPDC_SDDO12	source Driver Data	ENET2_TX_DATA1	+3,3V
-	45	EPDC_SDDO13	source Driver Data	ENET2_TX_EN	+3,3V
-	53	EPDC_SDDO14	source Driver Data	ENET2_TX_CLK	+3,3V
-	41	EPDC_SDDO15	source Driver Data	ENET2_RX_ER	+3,3V

Table 17

5.11 RESISTIVE TOUCH SCREEN

TSC is responsible for providing control of ADC and touch screen analogue block to form a touch screen system, which achieves function of touch detection and touch location detection. The controller utilizes ADC hardware trigger function and control switches in touch screen analogue block.

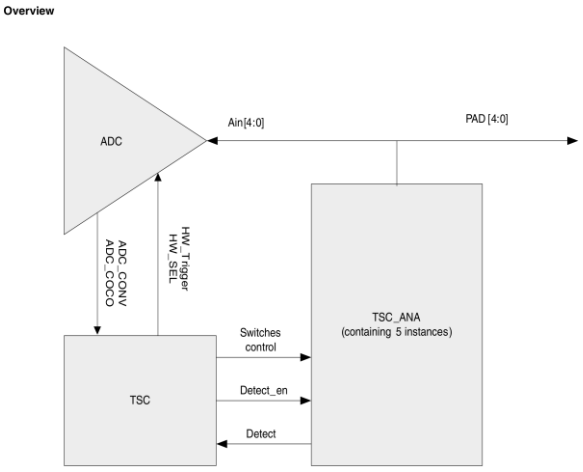


Figure 17

A Connector	Name	TSC Function Description	CPU Pin Name	GPIO Capable	Voltage
3	OSC_32KHZ_OUT	Touch Screen_XR	GPIO1_IO03	Y	+3,3V
27	GPIO1_IO04	Touch Screen_XL	GPIO1_IO04	Y	+3,3V
34	GPIO1_IO02	Touch Screen_YU	GPIO1_IO02	Y	+3,3V
48	I2C2_SDA	Touch Screen_YD	GPIO1_IO01	Y	+3,3V

Table 18

Note: for details and features see i.MX 6ULL reference Manual

5.12 BOOT MODE PIN

Boot mode pins 47, 49 of the A Connector determines how the module boot. The following table lists the possible options of the boot mode:

BOOT_MODE1 (PIN 49)	BOOT_MODE0 (PIN 47)	Action
0	0	Boot From Fuses
0	1	Serial Downloader
1	0	Internal Boot **(DEFAULT)**
1	1	Reserved

Table 19

BOOT_MODE 0 pin has a 10K pull-down on module
BOOT_MODE 1 pin has a 10K pull-up on module

The signal used to configure the boot is implemented on pin 89. In the standard condition the signal is setting to boot from internal module memory device (jumper left open), closing the jumper the module start from SD card.

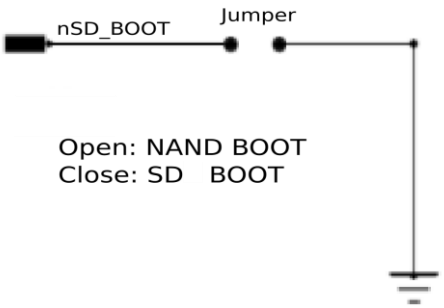


Figure 18

Following you can see the signals logical level to implement a custom starting sequence. The first sequence is already implemented in the module.

A Connector		
PIN	**nSD_BOOT**	
89	0	Boot from SD
	1	Boot From NAND

Table 20

Note: for using of any customized boot options refer to the NXP reference manual of i.MX6ULL

5.12.1 BOOT SIGNALS MANAGEMENT

Following are shown the signals you must consider during the boot sequence:

B Connector Pin Number	Signal	Status on Reset (Mandatory)	PIN constrained on Module	Boot Config Signal	Boot eFUSE Descriptions
26	DISP0_D0	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG1[0]	
24	DISP0_D1	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG1[1]	
16	DISP0_D2	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG1[2]	
18	DISP0_D3	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG1[3]	
22	DISP0_D4	Floating (High Impedance)	10K Ohm Pull Up	BOOT_CFG1[4]	
30	DISP0_D5	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG1[5]	
28	DISP0_D6	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG1[6]	
36	DISP0_D7	Floating (High Impedance)	10K Ohm Pull Up	BOOT_CFG1[7]	
20	DISP0_D8	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG2[0]	
14	DISP0_D9	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG2[1]	
2	DISP0_D10	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG2[2]	
6	DISP0_D11	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG2[3]	
8	DISP0_D12	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG2[4]	
10	DISP0_D13	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG2[5]	
12	DISP0_D14	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG2[6]	
4	DISP0_D15	Floating (High Impedance)	10K Ohm Pull Down	BOOT_CFG2[7]	
51	GPIO3_28	Floating (High Impedance)	-	BOOT_CFG4[0]	
47	GPIO3_27	Floating (High Impedance)	-	BOOT_CFG4[1]	
3	UART8_RXD	Floating (High Impedance)	-	BOOT_CFG4[2]	
1	UART8_TXD	Floating (High Impedance)	-	BOOT_CFG4[3]	
49	GPIO3_24	Floating (High Impedance)	-	BOOT_CFG4[4]	
39	GPIO3_23	Floating (High Impedance)	-	BOOT_CFG4[5]	
34	DISP0_D17	Floating (High Impedance)	-	BOOT_CFG4[6]	
32	DISP0_D16	Floating (High Impedance)	-	BOOT_CFG4[7]	

Table 21

The NXP documentation declares the above signals as BOOT_CFG signals but no other information (function and reset status) is currently given about them.
Basing on the Engicam test result we currently suggest leaving all these signals floating during reset status and **it's strongly recommended to consult the NXP's documentation before starting the carrier board design.**

WARNING:
The BOOT_CFG4 signals are used also to configure the boot from serial ROM, always refer to the NXP's documentations to design and configure the listed BOOT_CFG signals of your own board

5.13 HOW TO CONNECT THE AUDIO INTERFACE

The figure shows how to connect the module I2S interface to a low-power stereo codec, e.g. NXP SGTL5000, that includes headphones and is designed to provide a comprehensive audio solution for portable products that require line-in, mic-in, line-out, headphone-out and digital I/O.

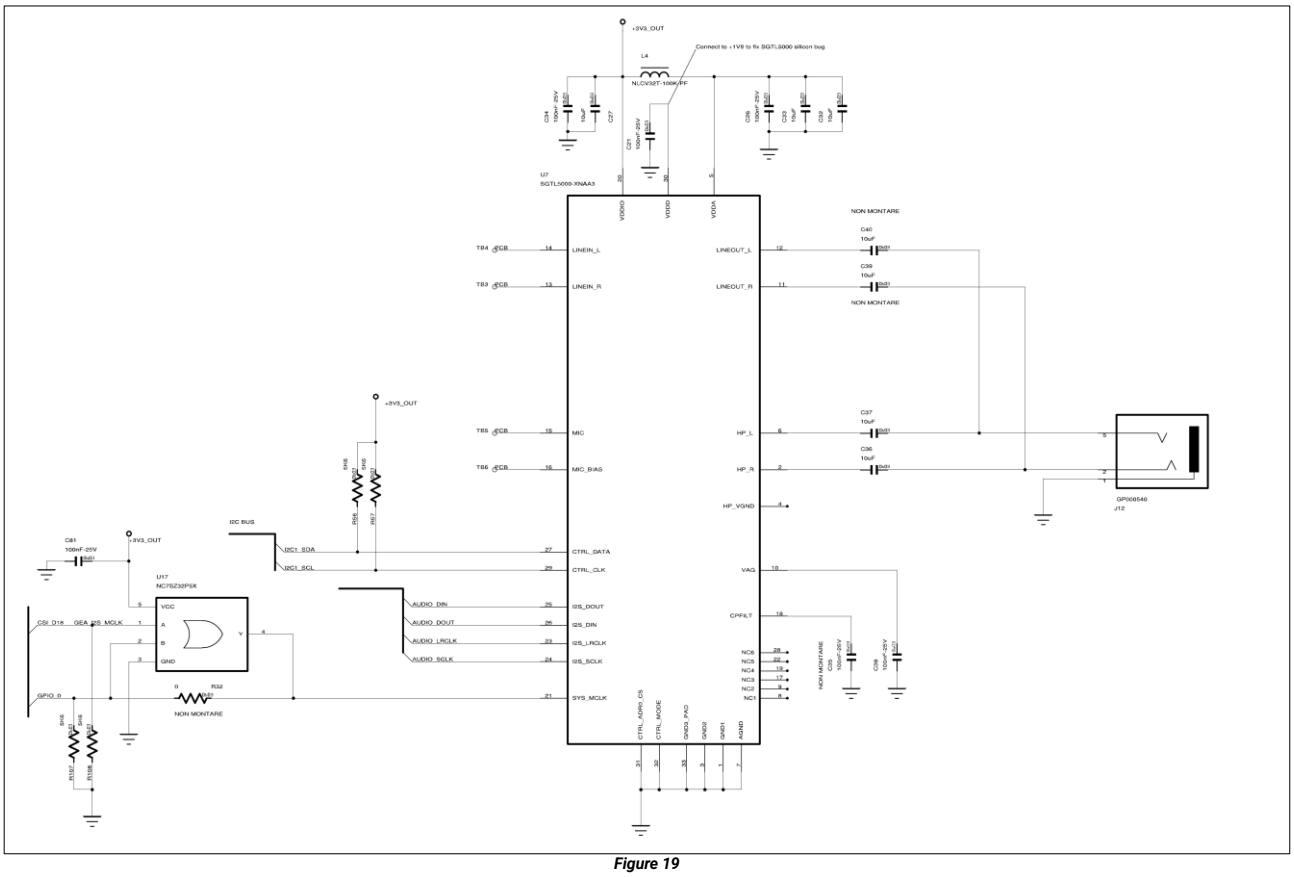


Figure 19

Following the I2S BUS pins mapping

A Connector	Name	Primary Function Description	Pin Name on i.MX	GPIO Capable	Voltage
53	I2S_DIN	I2S Data In	JTAG_TCK	Y	+3,3V
55	I2S_DOUT	I2S_Data OUT	JTAG_TRST_B	Y	+3,3V
59	I2S_SCLK	I2S_SCLK	JTAG_TDI	Y	+3,3V
57	I2S_LRCLK	I2S_LRCLK	JTAG_TDO	Y	+3,3V

Table 22

WARNING!
To implement the SGTL5000 on the carrier board, remember to supply the VDD pin 30 of the SGTL5000 device by fixed voltage as suggested to fix a silicon bug (for further detail refer to SGTL5000 data sheet)

5.14 HOW TO CONNECT THE RESET PIN

The nRESET signal Pin 85 on A connector, has input functionality and shall be driven in open-drain mode. *The signal has an internal 10K pull-up and 50-Ohm series resistors; the maximum recommended capacitive load is about 220 n**F**.*

By default, an active state on reset signal causes a COLD reset with a complete new power sequence (power off followed by a new power on).

This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).

If used, the reset pin shall be connected to an open-collector driver. If not used, leave floating.

CHAPTER 6

6. PERIPHERAL MULTIPLEXING

This Chapter gives the alternative peripheral information

Section includes：

- ✓ **I2S**
- ✓ **SPI**
- ✓ **PWM**
- ✓ **I2C**
- ✓ **UART**
- ✓ **CSI**
- ✓ **SD**
- ✓ **CAN**

6.1 PERIPHERAL MULTIPLEXING DESCRIPTION

Following we describe opportunity to use alternative interfaces using the properties of multiplexing pin.
Refer to the NXP's reference manual and documentation for further details.

6.1.1 SPI INTERFACES

Using pin multiplexing 's features we may have the following SPI and IIS connections. The tables below show the output signals on the Connector's module.

ECSPI1 signals interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
-	47	-	LCD_DATA22	MOSI	+3,3V
	72		CSI_DATA06		
-	51	-	LCD_DATA23	MISO	+3,3V
	74		CSI_DATA07		
-	1	-	LCD_DATA20	SCLK	+3,3V
	68		CSI_DATA04		
-	3	-	LCD_DATA21	SS0	+3,3V
	70		CSI_DATA05		
-	30	-	LCD_DATA05	SS1	+3,3V
-	28	-	LCD_DATA06	SS2	+3,3V
-	36	-	LCD_DATA07	SS3	+3,3V

Table 23

ECSPI2 signals interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
75	83	UART5_TX_DATA	CSI_DATA02	MOSI	+3,3V
73	81	UART5_RX_DATA	CSI_DATA03	MISO	+3,3V
7	79	UART4_TX_DATA	CSI_DATA00	SCLK	+3,3V
9	77	UART4_RX_DATA	CSI_DATA01	SS0	+3,3V
-	38	-	LCD_HSYNC	SS1	+3,3V
-	40	-	LCD_VSYNC	SS2	+3,3V
-	61	-	LCD_RESET	SS3	+3,3V

Table 24

ECSPI3 signals interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
71	-	UART2_CTS_B	-	MOSI	+3,3V
-	59	-	NAND_CE1		
69	-	UART2_RTS_B	-	MISO	+3,3V
65	-	UART2_RX_DATA	-	SCLK	+3,3V
67	-	UART2_TX_DATA	-	SS0	+3,3V

Table 25

6.1.2 IIS CONFIGURATION

The following tables show the pin configurations for IIS Bus on module's connector.

IIS1 bus interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
-	18	-	LCD_DATA03	I2S_DIN	+3,3V
-	72	-	CSI_DATA06		
-	22	-	LCD_DATA04	I2S_DOUT	+3,3V
-	74	-	CSI_DATA07		
-	16	-	LCD_DATA02	I2S_SCLK	+3,3V
-	70	-	CSI_DATA05		
-	24	-	LCDIF_DATA01	I2S_LRCLK	+3,3V
-	68	-	CSI_DATA04		

Table 26

IIS2 bus interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
53	-	JTAG_TCK	-	I2S_DIN	+3,3V
55	-	JTAG_TRST	-	I2S_DOUT	+3,3V
59	-	JTAG_TDI	-	I2S_SCLK	+3,3V
57	-	JTAG_TDO	-	I2S_LRCLK	+3,3V

Table 27

IIS3 bus interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
-	12	-	LCD_DATA14	I2S_DIN	+3,3V
-	40	-	LCD_VSYNC		
-	4	-	LCD_DATA15	I2S_DOUT	+3,3V
-	61	-	LCD_RESET		
-	10	-	LCD_DATA13	I2S_SCLK	+3,3V
-	38	-	LCD_HSYNC		
-	8	-	LCD_DATA12	I2S_LRCLK	+3,3V
-	42	-	LCD_ENABLE		

Table 28

6.1.3 ALTERNATIVE PWM PINS TABLE

It's possible to set the pins shown in the following table as PWM signals.

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
35	26	GPIO_IO08	LCD_DATA00	PWM-1	+3,3V
25	24	GPIO_IO09	LCD_DATA01	PWM-2	+3,3V
27	16	GPIO_IO04	LCD_DATA02	PWM-3	+3,3V
33	18	GPIO_IO05	LCD_DATA03	PWM-4	+3,3V
-	39	-	LCD_DATA18	PWM-5	+3,3V
	67	-	NAND_DQS		
59	49	JTAG_TDI	LCD_DATA19	PWM-6	+3,3V
53	85	JTAG_TCK	CSI_VSYNC	PWM-7	+3,3V
52	87	ENET1_RX_ER	CSI_HSYNC	PWM-8	+3,3V
55		JTAG_TRST			

Table 29

6.1.4 IIC CONFIGURATION

IIC1 Interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
7	62	UART4_TX_DATA	CSI_PIXCLK	I2C1_SCL	+3,3V
34	-	GPIO1_IO02	-		
3	64	GPIO1_IO03	CSI_MCLK	I2C1_SDA	+3,3V
9	-	UART4_RX_DATA	-		

Table 30

IIC2 Interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
30	87	GPIO1_IO00	CSI_HSYNC	I2C2_SCL	+3,3V
75	-	UART5_TX_DATA	-		
48	85	GPIO1_IO01	CSI_VSYNC	I2C2_SDA	+3,3V
73	-	UART5_RX_DATA	-		

Table 31

IIC3 Interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
28	24	UART1_TX_DATA	LCD_DATA01	I2C_SCL	+3,3V
-	55	-	ENET2_RX_DATA0		
26	26	UART1_RX_DATA	LCD_DATA00	I2C_SDA	+3,3V
-	37	-	ENET2_RX_DATA1		

Table 32

IIC4 Interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
67	18	UART2_TX_DATA	LCD_DATA03	I2C_SCL	+3,3V
-	35	-	ENET2_RX_EN		
65	16	UART2_RX_DATA	LCD_DATA02	I2C_SDA	+3,3V
-	43	-	ENET2_TX_DATA0		

Table 33

6.1.5 ALTERNATIVE UART PINS TABLES

The following tables shows an alternative UART configuration

UART1 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
-	11	-	GPIO1_IO06	UART1_CTS (Output)	+3,3V
-	75	-	UART1_CTS_B		
-	9	-	GPIO1_IO07	UART1_RTS (Input)	+3,3V
-	73	-	UART1_RTS_B		
28	-	GPIO1_IO00	-	UART1_TXD (Output)	+3,3V
34	-	GPIO1_IO02	-		
3	-	GPIO1_IO03	-	UART1_RXD (Input)	+3,3V
26	-	UART1_RX_DATA	-		

Table 34

UART2 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
2	-	UART3_TX_DATA	-	UART2_CTS (Output)	+3,3V
71	-	UART2_CTS_B	-		
36	-	UART3_RX_DATA	-	UART2_RTS (Input)	+3,3V
69	-	UART2_RTS_B	-		
67	-	UART2_TX_DATA	-	UART2_TXD (Output)	+3,3V
65	-	UART2_RX_DATA	-	UART2_RXD (Input)	+3,3V

Table 35

UART3 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
88	59	UART3_CTS_B	NAND_CE1	UART3_CTS (Output)	+3,3V
90	-	UART3_RTS_B	-	UART3_RTS (Input)	+3,3V
2	-	UART3_TX_DATA	-	UART3_TXD (Output)	+3,3V
36	-	UART3_RX_DATA	-	UART3_RXD (Input)	+3,3V

Table 36

UART4 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
-	38	-	LCD_HSYNC	UART4_CTS (Output)	+3,3V
-	40	-	LCD_VSYNC	UART4_RTS (Input)	+3,3V
7	-	UART4_TX_DATA	-	UART4_TXD (Output)	+3,3V
9	-	UART4_RX_DATA	-	UART4_RXD (Input)	+3,3V

Table 37

UART5 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
25	81	GPIO1_IO09	CSI_DATA03	UART5_CTS (Output)	+3,3V
-	83	-	CSI_DATA02	UART5_RTS (Input)	+3,3V
27	79	GPIO1_IO04	CSI_DATA00	UART5_TXD (Output)	+3,3V
75	-	UART5_TX_DATA	-		
33	77	GPIO1_IO05	CSI_DATA01	UART5_RXD (Input)	+3,3V
73	-	UART5_RX_DATA	-		

Table 38

UART6 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
-	87	-	CSI_HSYNC	UART6_CTS (Output)	+3,3V
-	85	-	CSI_VSYNC	UART6_RTS (Input)	+3,3V
-	55	-	ENET2_RX_DATA0	UART6_TXD (Output)	+3,3V
-	64	-	CSI_MCLK		
-	37	-	ENET2_RX_DATA1	UART6_RXD (Input)	+3,3V
-	62	-	CSI_PIXCLK		

Table 39

UART7 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
-	26	-	LCD_DATA06	UART7_CTS (Output)	+3,3V
52	-	ENET1_RX_ER	-	UART7_RTS (Input)	+3,3V
-	32	-	LCD_DATA16	UART7_TXD (Output)	+3,3V
-	35	-	ENET2_RX_EN		
-	34	-	LCD_DATA17	UART7_RXD (Input)	+3,3V
-	43	-	ENET2_TX_DATA0		

Table 40

UART8 interfaces

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
-	22	-	LCD_DATA04	UART8_CTS (Output)	+3,3V
-	53	-	ENET2_TX_CLK		
-	30	-	LCD_DATA05	UART8_RTS (Input)	+3,3V
-	41	-	ENET2_RX_ER		
-	1	-	LCD_DATA20	UART8_TXD (Output)	+3,3V
-	57	-	ENET2_TX_DATA1		
-	3	-	LCD_DATA21	UART8_RXD (Input)	+3,3V
-	45	-	ENET2_TX_EN		

Table 41

6.1.6 SD INTERFACES

SD1

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
3	70	GPIO1_IO03	CSI_DATA05	SD1_CD	+3,3V
-	73	-	UART1_RTS		
-	84	-	SD1_DATA0	SD1_D0	+3,3V
-	80	-	SD1_DATA1	SD1_D1	+3,3V
-	82	-	SD1_DATA2	SD1_D2	+3,3V
-	78	-	SD1_DATA3	SD1_D3	+3,3V
-	86	-	SD1_CLK	SD1_CLK	+3,3V
-	88	-	SD1_CMD	SD1_CMD	+3,3V

Table 42

SD2

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
-	9	-	GPIO1_IO07	SD2_CD	+3,3V
-	64	-	CSI_MCLK		
-	73	-	UART1_RTS_B		
-	1	-	LCD_DATA20	SD2_D0	+3,3V
-	79	-	CSI_DATA00		
-	3	-	LCD_DATA21	SD2_D1	+3,3V
-	77	-	CSI_DATA01		
-	47	-	LCD_DATA22	SD2_D2	+3,3V
-	83	-	CSI_DATA02		
-	51	-	LCD_DATA23	SD2_D3	+3,3V
-	81	-	CSI_DATA03		
-	49	-	LCD_DATA19	SD2_CLK	+3,3V
-	85	-	CSI_VSYNC		
-	39	-	LCD_DATA18	SD2_CMD	+3,3V
-	87	-	CSI_HSYNC		

Table 43

6.1.7 ALTERNATIVES CAN BUS INTERFACES

CAN 1 BUS Interface [1)]

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
88	20	UART3_CTS_B	LCD_DATA08	CAN1_TX	+3,3V
-	84	-	SD1_DATA0		
90	14	UART3_RTS_B	LCD_DATA09	CAN1_RX	+3,3V

Table 44

CAN 2 BUS Interface [1) 2)]

Pin on connector A	Pin on connector B	Pin Name on i.MX		MicroGEA Signal reference	Voltage reference
71	2	UART2_CTS_B	LCD_DATA10	CAN2_TX	+3,3V
-	82	-	SD1_DATA2		
69	6	UART2_RTS_B	LCD_DATA11	CAN2_RX	+3,3V
-	78	-	SD1_DATA3		

Table 45

[1)] ***Note: both the CAN BUS interfaces are not available on processor MCIMX6Y7***

[2)] ***Note: the CAN 2 BUS interface is not available on processor MCIMX6Y1 series***

ON-LINE SUPPORT

We offer an on-line support to allow the customer to stay updated on the development of software release and on the enhancement of the documentation.

Following is shown the references for ENGICAM on-line support.

ENGICAM Product Experts are available to answer questions via email:

support@engicam.com

PRODUCT COMPLIANCE

In order to respect own internal policy regarding the environmental regulations and safety laws, Engicam confirms the compliant, of this product to the normatives ROHS and REACH and to the recognized hazards.

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